The Propagation Group

ECL Design Guide

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Introduction

Emitter-Coupled Logic (ECL) ICs are ideal for operating in the gigahertz range due to their picosecond propagation delays. Additionally, thanks to their use of differential inputs, they are able to drive long transmission lines in relatively noisy environments while maintaining signal integrity. However, ECL devices impose special design considerations. First, due to their high speed operation at up to several Gigahertzes, designers must take into account transmission line effects which can severely disrupt propagating signals. Secondly, ECL chips are designed to be used with negative supplies. While it is possible to use them with positive supplies, designers must be extra careful of coupling noise onto V_{CC}.

Power Supplies

ECL outputs are referenced to the most positive supply rail [1]. This means that any noise appearing on the most positive supply rail will be directly coupled onto the output signal. For example, if the power supply is 5V and GND, then all outputs would be referenced to 5V, and any noise on the 5V supply would also be seen at the ECL outputs. Therefore, the older literature calls for ECL chips to be powered by a negative power supply, such as -5V and GND [1]. By using GND as the most positive supply rail, it is easier to maintain cleaner signals at the ECL outputs. GND is generally found to be less noisy as compared to a non-GND potential. This does not mean it is impossible to use a positive power supply. It does mean that precautions must be taken to ensure very little noise is coupled onto the most positive supply rail in order to maintain clean outputs.

As a note, when designing with ECL and positive supplies, it is called positive ECL (PECL) [1]. Likewise designing with negative supplies is called Motorola ECL (MECL) design, or more commonly and intuitively, negative ECL (NECL) [1]. The ‘P’, ‘M’, or ‘N’ prefix merely describes the power supply configuration. It has no effect on the devices themselves [1]. An ECL device is a PECL device is a NECL device.

Input/Output Configurations

ECL uses two input/output (I/O) configurations: single-ended and differential. Single-ended I/O is generally easier to implement, but differential I/O exhibits greater immunity to noise. It is important to note that for both single-ended and differential devices, $V_{IH/OH}$ and a $V_{IL/OL}$ do not correspond to the upper and lower supply rails, though as aforementioned, they are coupled to the upper rail. Table 1 shows how V_{OH} and V_{OL} are generated relative to V_{CC}. Additionally, Table 2 shows $V_{IH/OH}$ and a $V_{IL/OL}$ given a 10E type ECL device using a PECL setup (V_{CC} = 5.0V, V_{EE} = GND) operating at 25°C. Note V_{BB}, which is the bias voltage of a differential input. This is used for connecting single-ended outputs to differential inputs, and will be explained further in a later section. Also note that voltage swing for an ECL output is 800mV, and this voltage swing is roughly centered on VBB.

Single-ended I/O is similar in function to the I/O used in CMOS and TTL. To determine if the signal is a ‘1’ or ‘0’, the input voltage is compared to a threshold voltage. If the input voltage is greater than the threshold, it is declared a ‘1’; if the

input voltage is less than the threshold, it is declared a '0'. For ECL, this threshold voltage is VBB.

Table 1. ECL I/O Ranges (in Volts) Relative to V_{CC} [1]

Symbol	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{BB}
Max	V_{CC} – 0.81	V_{CC} – 1.63	V_{CC} – 0.81	V_{CC} – 1.48	V_{CC} – 1.25
Min	V_{CC} – 0.98	V_{CC} – 1.95	V_{CC} – 1.13	V_{CC} – 1.95	V_{CC} – 1.35

Table 2. PECL I/O Ranges (in Volts) with V_{CC} = 5.0V [1]

Symbol	V_{OH}	V_{OL}	V_{IH}	V_{IL}	V_{BB}
Max	4.19	3.37	4.19	3.52	3.75
Min	4.02	3.05	3.87	3.05	3.65

The differential I/O significantly reduces noise at the input through common-mode rejection [2]. Each differential input takes in two signals, and likewise each differential output emits two signals. The two signals together are known as a differential pair [2]. One of the signals is referred to as the "true" signal, and the other is the "inverted" signal [2]. The difference of these signals ("true" minus "inverted") distinguishes a binary '1' from '0':

$$1: V_{Diff,True} - V_{Diff,Inverted} > 0$$

$$0: V_{Diff,True} - V_{Diff,Inverted} < 0$$

When connecting a differential output to a differential input, the wires or traces connecting the differential pair should be run adjacent to each other. Ideally, this will cause any noise coupled onto one of the signals to be coupled onto the other. When the differential input "subtracts" the inverted signal voltage from the true signal voltage, the noise will be removed. That is, any signal common to the differential pair (in this case noise) will be rejected.

Termination of ECL Devices

ECL outputs are bipolar junction transistors (BJT) configured as emitter followers [3]. To maintain their fast switching rates, these emitter followers should operate in the forward active region at all times, requiring them to source current at all times [3]. ECL inputs have large impedance (typically around 75 kΩ) that does not allow for the necessary current sourcing by the ECL output [3]. Instead, this current sourcing is achieved by terminating the ECL output through a resistor, R_t, to a voltage, V_{TT}, such that

$$V_{TT} = V_{CC} - 2.0V$$
$$R_t = Z_0$$

where Z_0 is the characteristic impedance of the transmission line connecting the ECL output to R_t [3]. ECL outputs are typically 50Ω, thus the terminating resistor as well as the transmission line's characteristic should be approximately 50Ω [3].

There are two preferred termination schemes for ECL devices. One scheme, called "parallel termination", terminates any signal carrying line via a resistor, R_T, to a supply operating at V_{TT} [3]. The other, called "Thevenin parallel termination", involves a Thevenin equivalent circuit that creates a termination voltage and resistance equivalent to V_{TT} and R_T [3].

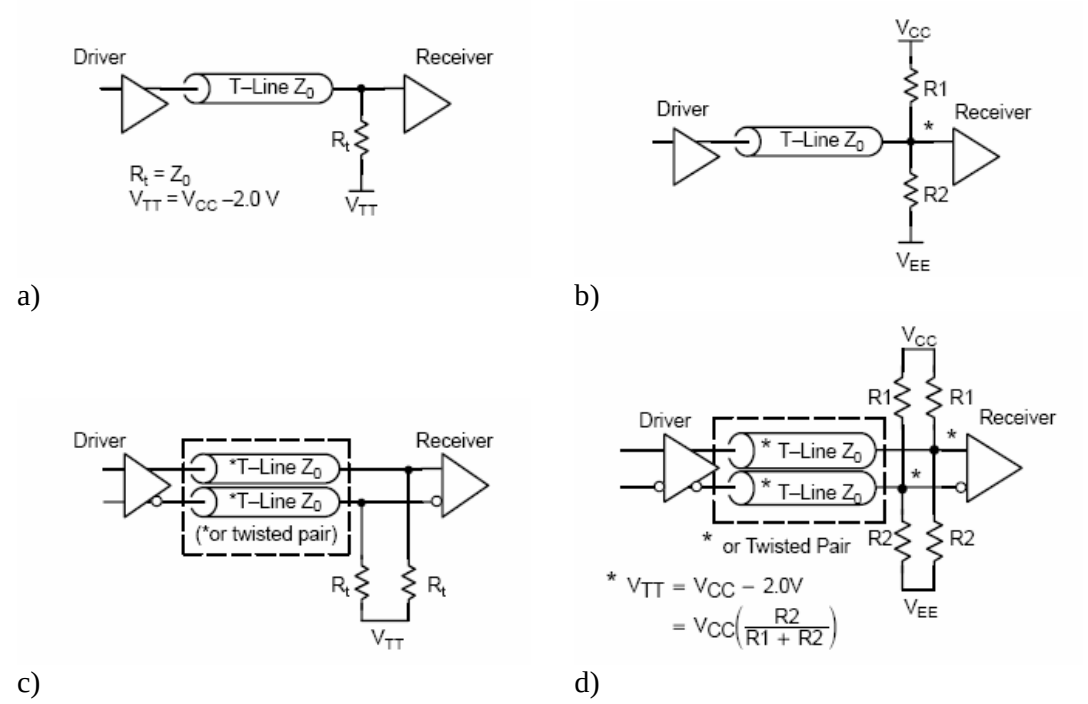

Figure 1. Termination schemes for I/O interfaces: a) single-ended parallel, b) single-ended Thevenin parallel, c) differential parallel, d) differential Thevenin parallel [3].

Thevenin Parallel termination, while avoiding the need for a secondary supply, consumes additional power as compared to parallel termination [3]. Conversely, parallel termination consumes less power, but requires a supply operating at V_{TT} [3]. An additional point to note is that for the Thevenin parallel termination, any noise on V_{CC} is partially coupled onto V_{TT} [3.

The most important factor when using ECL devices is to be sure that their output emitter follower always operates in the forward active region [3]. Fluctuations in the supply voltages V_{CC} and V_{TT} may cause V_{OL} to be less than or equal to V_{TT}, which would make I_{OL} = 0 mA and place the emitter follower in cutoff. This would increase the propagation delay of the device due to the time required to pull the emitter follower out of the cutoff state. Therefore, it is necessary to ensure V_{OL} always remains greater than V_{TT}.

The partial coupling of V_{CC} onto V_{TT} for the Thevenin parallel termination helps to keep $V_{OL} > V_{TT}$. This combined with the single supply design make it the preferred

termination scheme for ECL devices, even though it imposes greater power requirements [3].

As a final note on terminations, placement of the termination circuit is important. When connecting an output on device A to an input on device B, the termination circuit should be implemented as close as possible to the input on device B [3].

Differential and Single-Ended ECL I/O and Interfacing

Both differential and single-ended I/O are popular interfacing schemes, resulting in four possible configurations.

Differential Output to Differential Input
For interfacing a differential output to a differential input, connect the true and inverted outputs directly to the corresponding true and inverted inputs [3]. Then, apply the preferred termination scheme [3].

Single-ended Output to Single-ended Input
Single-ended I/O is just as straightforward: connect the signal output to the signal input and apply the preferred termination scheme [3].

Differential Output to Single-ended Input
For interfacing a differential output to a single-ended input, connect the true output to the single-ended input and apply the preferred termination [4]. The inverted output should also be terminated in a manner similar to the true output, even though it is not connected to another device [4].

Single-ended Output to Differential Input
For interfacing a singled-ended output to a differential input, the general design rule becomes more complicated depending on the devices used. Recall that the binary value of a differential input is determined by the difference of the true and inverted input voltages. The signal output should be connected to the true input of the differential device [4]. To make the differential device function correctly, the inverted input should be connected to a threshold voltage equivalent to $(V_{IH} + V_{IL})/2$ [4]. A quick comparison of V_{BB} to V_{IH} and V_{IL} in Table 1 and 2 shows that V_{BB} is not exactly midpoint voltage. However, VBB is still used for as a threshold voltage.

If a V_{BB} pin is available on a device (i.e., MC10EP16) than it may be connected directly to the inverted pin of the ECL differential input on that device [4]. V_{BB} is not a typical ECL output but rather a current source/sink. Therefore, it is not necessary to terminate V_{BB} to V_{TT} via some termination scheme. However, V_{BB} should be decoupled from V_{CC} via a small capacitance. A typical value is 0.01 uF [4].

Not all differential input devices may have V_{BB} available on chip, and unfortunately, when unconnected, the inverted input pin generally defaults to $V_{CC}/2$ rather than V_{BB}. For devices without V_{BB}, it is necessary to generate the bias voltage externally and connect it to the inverted input. This can be done via a voltage divider network or a "16" type buffer device [4]. It may be necessary to buffer V_{BB} via an op-amp configured as a voltage follower to allow sufficient current sourcing/sinking. Further details on connecting single-ended and differential devices can be found in ON Semiconductor's application note "AND8020/D: Termination of ECL Logic Devices"

[3] as well as Maxim's application note "HFAN-1.0.1: Interfacing Single-Ended PECL to Differential PECL and Differential PECL to Single-Ended PECL" [4].

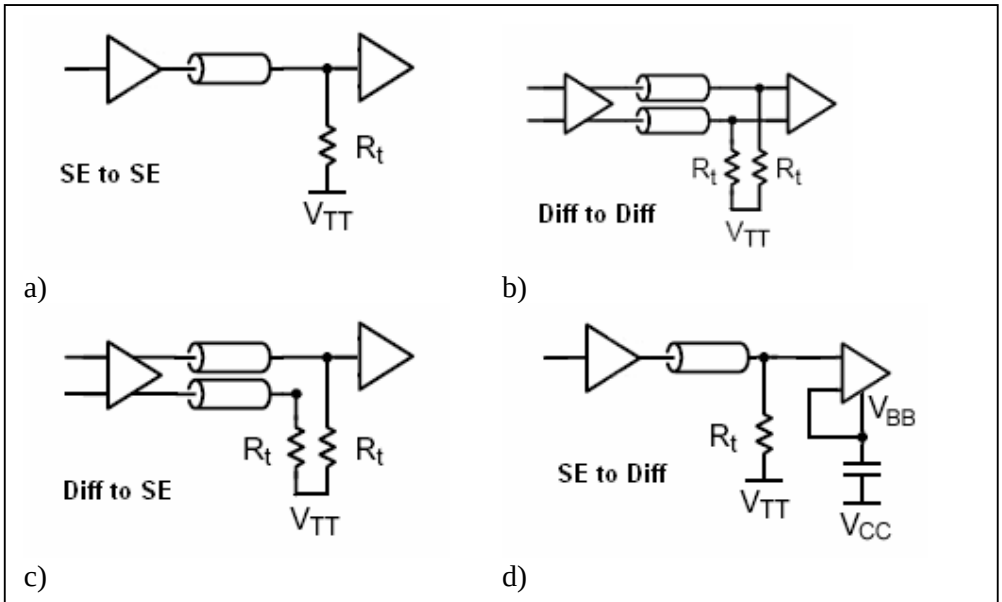

Figure 2. Interfacing various I/O (using parallel termination): a) single-ended output to single-ended input, b) differential output to differential input, c) differential output to single-ended input, d) single-ended output to differential input [3].

Interfacing to 50Ω Test Equipment

Many instruments feature high-impedance inputs, which allow the direct connection of a terminated ECL output. However, this is not ideal for monitoring an ECL output, especially when the distance between the ECL termination and the test equipment becomes substantial. Instruments with a 50Ω load are also not ideal for directly connecting ECL outputs, because they terminate through 50Ω to GND rather than V_{TT}.

One method of interfacing with a 50Ω load is shown in Figure 3 [5]. Resistor R_S provides the constant DC current sourcing while the 50Ω load in parallel with R_S provides the sink/source for the AC currents. Capacitor C should be large to provide an AC short from the ECL output to the test equipment, but the precise value is dependent on the circuit's clock frequency. For a 5V PECL system, an R_S of approximately 274Ω will cause the ECL output to source 22.76mA for V_{OH} and 3.8mA for V_{OL}. This corresponds well with the typical sourcing of 21.1mA and 5.1mA for V_{OH} and V_{OL} respectively when the ECL output is terminated through 50 Ω to V_{TT}.

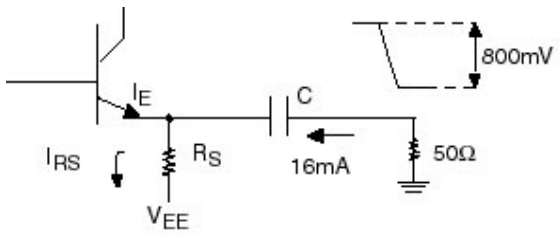

Figure 3. ECL output connected to a 50Ω coupled load [5].

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