1. Two logic gates are connected by a transmission line with the following circuit parameters:

\[ Z = 100 \, \Omega, \quad T = 50 \, \text{ns} \]

\[ 400 \, \text{pF} \]

\[ 5 \, \text{V} \]

\[ 2000 \, \Omega \]

Note that the logic gate being driven by the transmission line has 400 pF of parasitic capacitance. If a short logic pulse is sent down the line by closing switch A for a period of 30 ns, answer the following questions:

(a) Sketch the output \( V_L(t) \) for \( t \geq 0 \) s, clearly labeling all voltage levels and times. (3 points)

(b) If the logic pulse will not trigger a gate until a threshold of 2.5 V is exceeded at its input terminals, what is the total triggering latency (as measured from the origin of the pulse at \( t = 0 \)) for this transmission line? (2 points)

2. Below is a transmission line that drives a simple diode with the following V-I characteristic:

\[ V_L = V_0 \ln \left( \frac{I_L}{I_0} + 1 \right) \]

where \( V_0 = 0.4 \, \text{V} \) and \( I_0 = 0.5 \, \text{mA} \).
(a) Find the steady state load voltage and current. (3 points)

(b) Calculate the steady-state reflected voltage on the line. (2 points)

(c) Now reverse the diode at the end of the line and find the new steady state load voltage and current. (3 points)

(d) Calculate the steady-state reflected voltage on the line. (2 points)

3. Below is a chaotic transmission line circuit where $R_s$ can take on any value greater than $-32.5\Omega$. Find a source resistance value that leads to an output that oscillates between 3 distinct values. Plot the output.

\[
\begin{align*}
R_s & \quad 0.2 \, \text{V} \\
V_L & \quad \text{I}_L \\
Z_0 = 50 \, \Omega & \quad -
\end{align*}
\]