

# Curriculum Topic : Time-Domain Transmission Lines

## TDT4 : Termination Schemes

<i>Module Outline:</i>	
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### Prerequisite Skills

*Prerequisites / Requirements:*

**TDT3** Transmission Line Equations

### Competencies

**Competency TDT.4:** Understanding termination schemes for switched transmission lines.

*Competency Builders:*

- TDT.4.1 List the basic types of transmission line matching schemes for DC-switched signals.
- TDT.4.2 Understand the trade-offs between cost, complexity, and power consumption in the various termination schemes.
- TDT.4.3 Design a termination scheme for an arbitrary transmission line connection.

### Supplemental Reading and Resources

*Supplemental Reading Materials:*

A.F. Peterson and G.D. Durgin. *Transient Signals on Transmission Lines: An Introduction to the Non-Ideal Effects and Signal Integrity Issues in Electrical Systems*. Morgan & Claypool Publishers, 2009. Chapter 4.

## Assessments

The following questions and exercises may serve as either pre-assessment or post-assessment tests to evaluate student knowledge.

*Question:* TDT4.1

*Competency:* TDT.4.1

Name 4 types of termination schemes studied in the course.

*Answer:*

Series match, parallel match, capacitor match, diode match

*Question:* TDT4.2

*Competency:* TDT.4.2

Under what scenario might a parallel match be preferred to a capacitor match? Under what scenario might a capacitor match be preferred to a parallel match?

*Answer:*

The capacitor match is preferred with power consumption and dissipation is an issue, since the parallel match uses extra resistance – and, hence, extra power dissipation – to suppress reflections. The resistive parallel match may be preferred whenever a transmission line is driving a high-impedance load and the duration of the switched DC signals or pulses are unknown (since the capacitor selection in the capacitor match will make the signals time-constant dependent).

*Question:* TDT4.3

*Competency:* TDT.4.3

A 50- $\Omega$  transmission line drives a 500- $\Omega$  logic load and is itself driven by a 25- $\Omega$  logic output source. What would the source-side series matching resistor value be for this circuit? What would the load-side parallel matching resistor be for this circuit?

*Answer:*

The series match would require a 25- $\Omega$  resistor. The parallel match would require a 56- $\Omega$  resistor.