

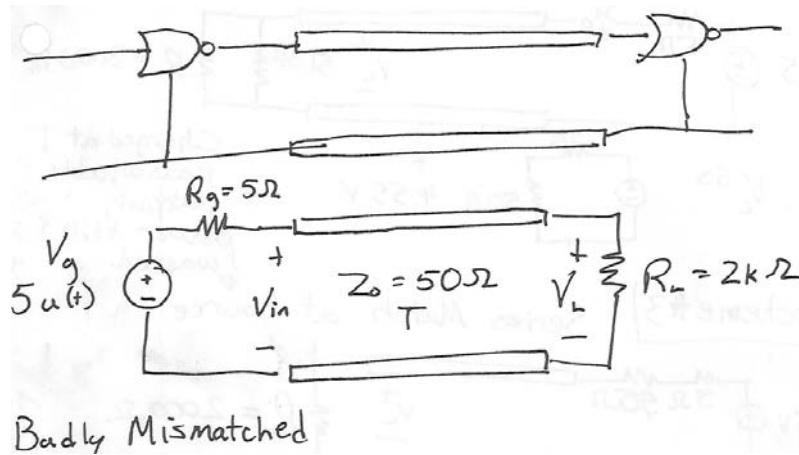
TDT4: Termination Schemes

By Prof. Gregory D. Durgin

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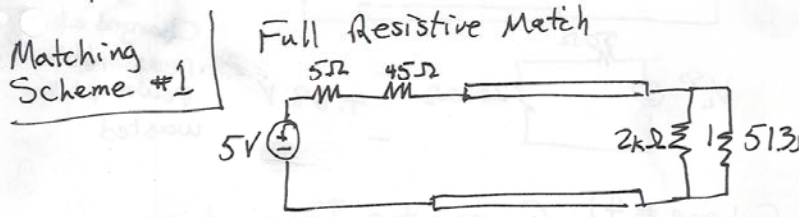
Badly Mismatched Logic Circuit



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Full Resistive Match



Match at both source and load \rightarrow Poor

a) $V_L^{ss} = 2.5V$ (not $4.998V$)

b) Power wasted across matching resistors

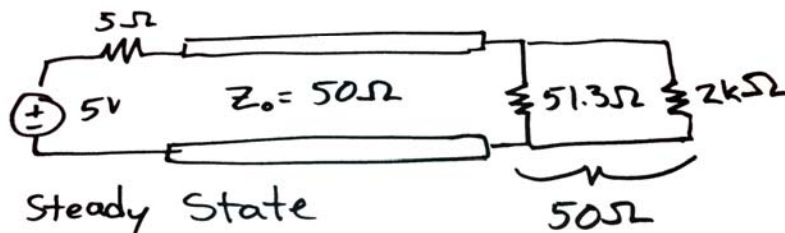
Need a better scheme

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Parallel Match at Load

Scheme 2 | Parallel Match at Load

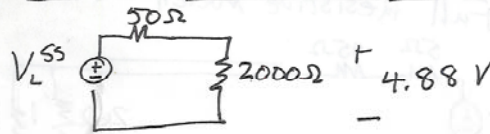
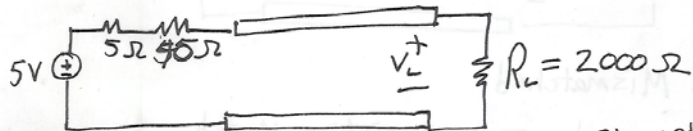


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Series Match at Source

Scheme #3 | Series Match at Source



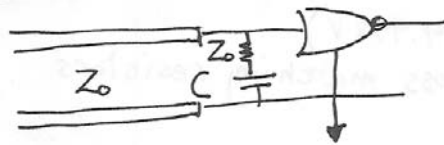
Charged at T ,
reasonable
power still
wasted

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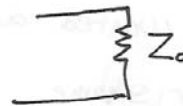


Capacitor Termination

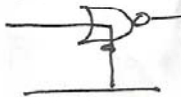
Scheme #4 | Capacitor Termination



at $t = T$,



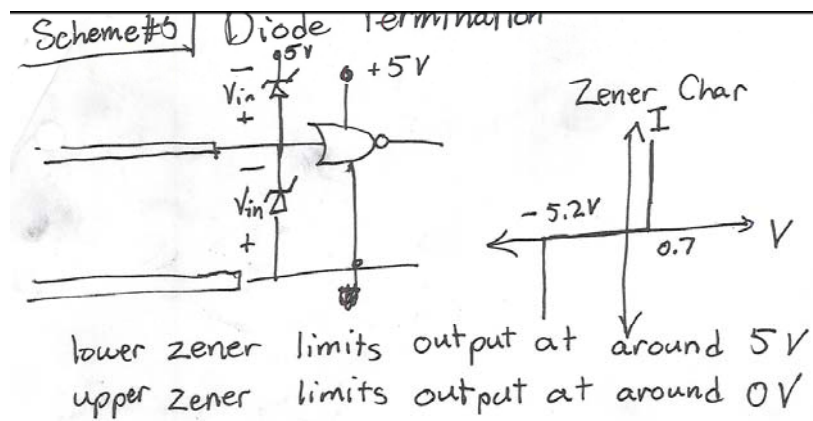
at $t \rightarrow \infty$



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Termination with Zener Diodes



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