Curriculum Topic :
Time-Domain Transmission Lines

TDT8 : Reactive Terminations on Transmission Lines

Module Outline:	
Prerequisite Skills	Competencies
Supplemental Reading and Resources	Assessments
Laboratory Activities	Power Point Slides and Notes

Prerequisite Skills

Prerequisites / Requirements:
TDT7 Short pulses on transmission lines

Competencies

Competency TDT.8: **Quantify the signal effects of a reactive load terminating a transmission line.**

Competency Builders:
TDT.8.1 Quantify the effects of a capacitive load on the end of a transmission line with DC pulses
TDT.8.2 Quantify the effects of an inductive load on the end of a transmission line with DC pulses

Supplemental Reading and Resources

Supplemental Reading Materials:

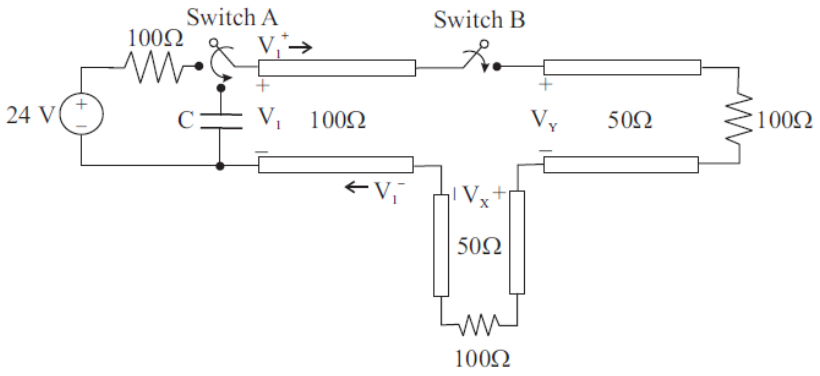
A.F. Peterson and G.D. Durgin. *Transient Signals on Transmission Lines: An Introduction to the Non-Ideal Effects and Signal Integrity Issues in Electrical Systems*. Morgan & Claypool Publishers, 2009. Chapter 8.

Assessments

The following questions and exercises may serve as either pre-assessment or post-assessment tests to evaluate student knowledge.

Question: TDT8.1 *Competency:* TDT.8.1

) **T-line Sequence Problem:** Below is a transmission line circuit. Fill out the state table as the circuit is sequentially switched under the following conditions. Note: V_1^+ is measured at the *start* of the first transmission line while V_1^- is measured at the *end* of the first transmission line. Assume ideal circuit components. (**44 points**)



- State 0: Both switches are open and both lines are uncharged.
- State 1: Immediately after switch A is closed onto the DC source.
- State 2: Switch A has been closed (connected to the source) for a while.
- State 3: Immediately after switch B is closed.
- State 4: Switch B has been closed for a while.
- State 5: Immediately after switch A closes onto the stand-alone capacitor.

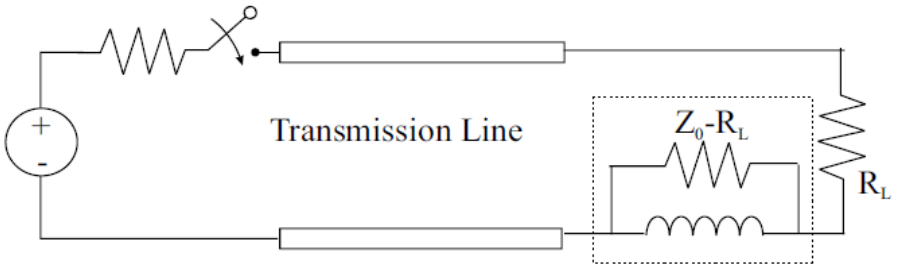
	V_1	V_X	V_Y	V_1^+	V_1^-
State 0	0	0	0	0	0
State 1		0	0		0
State 2					
State 3					
State 4					
State 5					

Answer:

	V_1	V_X	V_Y	V_1^+	V_1^-
State 0	0	0	0	0	0
State 1	12	0	0	12	0
State 2	24	0	0	12	12
State 3	24	6	6	12	0
State 4	16	8	8	12	4
State 5	0	8	8	-4	4

Question: TDT8.2 *Competency:* TDT.8.2

Mystery Matching Circuit: The dashed box below contains an unusual matching circuit for switched DC logic signals. Explain why this circuit matches the load, as well as any limitations on the values of R_L that can be used for this type of circuit.



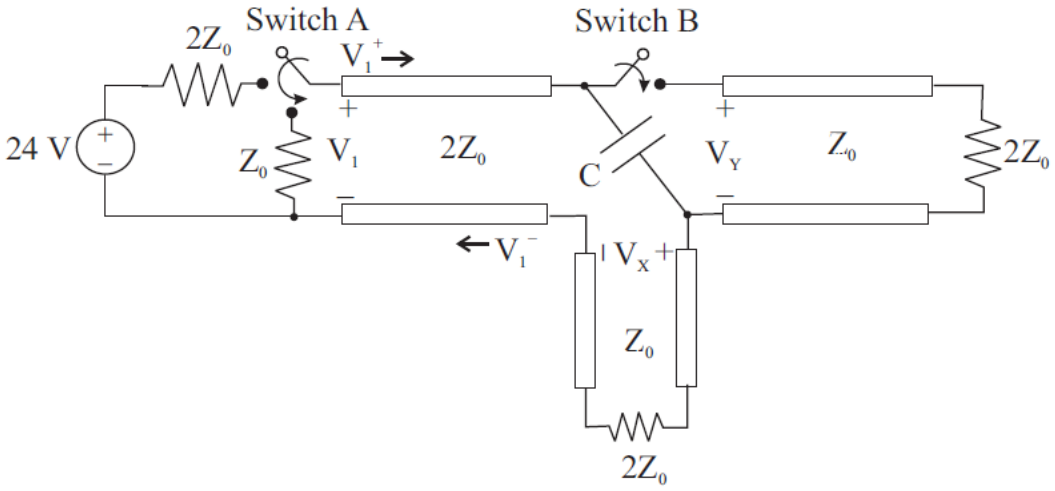
Answer:

The inductor acts as an open circuit initially, so that the load resistance appears to be $Z_0 - R_L$ in series with R_L for a total of Z_0 resistance – a perfect match to the line! In time the inductor becomes a short circuit, removing the effects of the matching resistor; only the true load remains. This scheme only works for $R_L < Z_0$ – otherwise, the matching resistor would have to be negative.

Question: TDT8.3 *Competency:* TDT.8.1

(4) **Switching Network:** The circuit below represents a high-speed digital interconnect that is switched according to the following states:

- State 0: Both switches are open and both lines are uncharged.
- State 1: Immediately after switch A is closed onto the DC source.
- State 2: Switch A has been closed for a while.
- State 3: Immediately after switch B is closed.
- State 4: Switch B has been closed for a while.
- State 5: Immediately after switch A closes onto the stand-alone Z_0 resistor.



Fill out the following table according to these switching states (skip state 3). Assume all backwards propagating waves are measured from the right-most side of the transmission line. Assume all forward propagating waves are measured from the left-most side of the transmission line. (**34 points**):

	V_1	V_X	V_Y	V_1^+	V_1^-
State 0	0	0	0	0	0
State 1		0	0		0
State 2					
State 4					
State 5					

Answer:

	V_1	V_X	V_Y	V_1^+	V_1^-
State 0	0	0	0	0	0
State 1	12	0	0	12	0
State 2	24	0	0	12	12
State 4	16	8	8	12	4
State 5	8/3	8	8	-4/3	4