Practice Questions for Test 1

ECPE 3025: Electromagnetics

Note: Below is a list of all reject test questions I compiled while writing the original test for this class. This document is only meant for practice. The questions on the in-class test ARE NOT as numerous as those contained by this document.

(1) Short Answer Section

- (d) ______(1) _____(2)
 In a network with switched DC excitation, capacitors look like <u>Answer 1</u> circuits initially, and <u>Answer 2</u> circuits in the steady state.
- (e) (1) (2)
 In a network with switched DC excitation, inductors look like Answer 1 circuits initially, and Answer 2 circuits in the steady state.
- (f) ______(1) _____(2) _____(3) There are three ways to increase Z₀ for a coaxial line. You could <u>Answer 1</u> the radius of the inner conductor, <u>Answer 2</u> the radius of the outer conductor, or <u>Answer 3</u> the permittivity of the dielectric material. (Use the words increase or decrease in these blanks.)

⁽g) ______ True or False: One way to eliminate crosstalk between two lines is to place lines further apart.

(h) _____

<u>Answer</u> is a computational technique for solving for voltages and currents in a circuit with nonlinear components.

(2) Descriptive Answer Section

(a) **Transmission Line Equations:** Below are solutions to a transmission line partial differential equation:

$$v(z,t) = V^{+}f\left(t - \frac{z}{v_{p}}\right) + V^{-}g\left(t + \frac{z}{v_{p}}\right)$$
$$i(z,t) = \frac{V^{+}}{Z_{0}}f\left(t - \frac{z}{v_{p}}\right) - \frac{V^{-}}{Z_{0}}g\left(t + \frac{z}{v_{p}}\right)$$

Perform the following analysis:

- In the equations above, circle the portion of the solution representing the backward-propagating voltage waveform.
- In the equations above, box the forward-propagating *amplitude* of the current waveform.
- Write a simplified expression for time-varying voltage evaluated at the front of the line (z = 0).
- Write a simplified expression for space-varying current on the line at $t = \frac{D}{v_p}$.

(b) Continuum of Reactance: Mona is a graduate TA for electronics lab. One day (when she has a little extra spare time) Mona notices two giant canisters in the corner of the lab: one contains thousands of 100 nF capacitors and the other contains thousands of 1 mH inductors. Out of sheer boredom, she connects all of the capacitors and inductors together to form a long, repetitive chain:



This chain is so long, it wraps around the Van Leer hallway for several hundred feet. She then hits the front of this device with a 100V-square pulse using an ideal (zeroimpedance) function generator. She hooks up numerous oscilloscopes and ammeters along the chain to observe what happens. Describe the behavior Mona observes, including numbers for the values of voltages and currents in the chain.

(c) Mystery Matching Circuit: The dashed box below contains an unusual matching circuit for switched DC logic signals. Explain why this circuit matches the load, as well as any limitations on the values of R_L that can be used for this type of circuit.



Work-out Problem Section

(3) **Discharge of a Long Capacitor:** As a practical joke, you charge up a long, skinny parallel-plate capacitor to 200 V and leave it in your friend's sock drawer. While charged, your friend begins rummaging for socks and touches the end of the capacitor with his 100Ω finger which happens to be perfectly matched to the transmission line model of these parallel plates:



How long does the discharge last? Draw sketches of the voltage across the length of the capacitor (as a function of position) for the following moments in time: t = 0, $t = \frac{T}{2}$, t = T, $t = \frac{3T}{2}$, and t = 2T.

(4) A circuit board with depth h between ground plane and surface etchings contains a stripline fanout that connects the output of chip 0's logic gate to the input logic gates of two other chips, as illustrated in the diagram below:



The values of h, w_0 , and ϵ_r are fixed board parameters. You may use the following approximations for input impedance and velocity of propagation on a stripline:

$$Z_0 = \frac{377}{\sqrt{\epsilon_r} \left[\frac{w}{h} + 2\right]} \qquad v_p = \frac{3 \times 10^8}{\sqrt{\frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + h/w}}}}$$

a. Solve for two trace width values w_1 and w_2 , in terms of fixed board parameters, that forward-match the circuit at the fanout junction (looking forward).

b. Describe how you might design the widths w_1 and w_2 so that impedance matches at the fanout junction (looking forward) and signals arrive at the gates of chips 1 and 2 at the exact same time. You do not have to solve for w_1 or w_2 , but you should specify conditions that Z_0 and v_p must satisfy.