ECE 3025: Electromagnetics

Solutions to TEST 1 (Spring 2008)

(1) **RFID on Metal Surfaces:**

(a) The reflected voltage will be +1 V for the open circuit load, -1 V for the short circuit load.

(b) Both open and short circuits result in a VSWR of ∞ dB.

(c) As the RFID tag is brought closer to a metal surface, this is equivalent to shrinking b in the microstrip transmission line model. Thus, the line becomes more capacitive and less inductive. Therefore, Z_0 drops.

(d) Start with the phasor solution for current and voltage on a transmission line:

$$\tilde{v}(z) = V^+ \exp(-j\beta z) + V^- \exp(+j\beta z) \qquad \tilde{i}(z) = \frac{V^+}{Z_0} \exp(-j\beta z) - \frac{V^-}{Z_0} \exp(+j\beta z)$$

Note that $I_S = \tilde{i}(z=0)$ and $I_L = \tilde{i}(z=D)$ and that, according to KCL, $I_S = I_L$ in the current loop that includes the RFIC. Thus, we may write

$$\frac{V^+}{Z_0} \exp(-j\beta 0) - \frac{V^-}{Z_0} \exp(+j\beta 0) = \frac{V^+}{Z_0} \exp(-j\beta D) - \frac{V^-}{Z_0} \exp(+j\beta D)$$

which simplifies to

$$\frac{V^-}{V^+} = \frac{1 - \exp(-j\beta D)}{1 - \exp(j\beta D)} = -\exp(-j\beta D)$$

(e) If you got the answer in part (d), the jump to a Thevenin equivalent impedance is not too difficult. The voltage across the terminals of the RFIC, if we do a KVL, is going to be $V_{th} = \tilde{v}(z=0) - \tilde{v}(z=D)$:

$$\tilde{v}(z) = V^+ \exp(-j\beta z) + (V^+ \cdot -\exp(-j\beta D)) \exp(+j\beta z)$$

$$V_{th} = V^+(1 - \exp(-j\beta D)) - V^+(\exp(-j\beta D) - 1) = 2V^+(1 - \exp(-j\beta D))$$

The corresponding current into the transmission line is

$$I_{th} = \frac{V^+}{Z_0}(1 + \exp(-j\beta D))$$

Finishing our computation,

$$Z_{th} = \frac{V_{th}}{I_{th}} = \frac{2Z_0(1 - \exp(-j\beta D))}{1 + \exp(-j\beta D)} = j2Z_0 \tan(\beta D/2)$$

Does this make physical sense? If the transmission line has length zero, then its Thevenin equivalent impedance is 0Ω, which makes sense. As length is added, the lossless transmission line in this topology appears to be an inductor, storing reactive power without permanently expending it.

(2) **PCB Reflections:**

One way to solve this problem is to simply list all the reflection combinations that produce a response at the input terminals of chip 2, noting the total transit times of each pathway. In the short-hand notation below, C1 $\rightarrow$ T $\rightarrow$ C3 $\rightarrow$ T $\rightarrow$ C2, denotes a pulse originating from chip 1 that travels to the T-junction, then travels to chip 3, where it is reflected back

to the T-junction and onward to chip 2.

- 6 ns (C1 → T → C2)
- 10 ns (C1 → T → C2 → T → C2)
- 14 ns (C1 → T → C2 → T → C2 → T → C2)
- 18 ns (C1 → T → C2 → T → C2 → T → C2 → T → C2)
- 22 ns (C1 → T → C2 → T → C2 → T → C2 → T → C2 → T → C2)
- 26 ns (C1 → T → C2 → T → C2 → T → C2 → T → C2 → T → C2 → T → C2)
- 16 ns (C1 → T → C2 → T → C3 → T → C2)
- 20 ns (C1 → T → C2 → T → C3 → T → C2 → T → C2)
- 24 ns (C1 → T → C2 → T → C3 → T → C2 → T → C2 → T → C2)
- 22 ns (C1 → T → C2 → T → C3 → T → C3 → T → C2)
- 26 ns (C1 → T → C2 → T → C3 → T → C3 → T → C2 → T → C2)
- 14 ns (C1 → T → C1 → T → C2)
- 18 ns (C1 → T → C1 → T → C2 → T → C2)
- 22 ns (C1 → T → C1 → T → C2 → T → C2 → T → C2)
- 26 ns (C1 → T → C1 → T → C2 → T → C2 → T → C2 → T → C2)
- 12 ns (C1 → T → C3 → T → C2)
- 16 ns (C1 → T → C3 → T → C2 → T → C2)
- 20 ns (C1 → T → C3 → T → C2 → T → C2 → T → C2)

Removing the repeating cases, the unique times when a pulse is registered at chip 2 are t =6, 10, 12, 14, 16, 18, 20, 22, 24, and 26 ns.

Another more elegant way to reason through this problem is to recognize that: a) only even integer values of t can possibly register a pulse (since the only line with an odd transit time of 3ns must reflect *down* and *back*, thereby accumulating an even 6 ns of total transit time) and b) if any pulse travels a total time t_0, then there also exist paths at $t_0 + 4n$ ns, where n is any positive integer, due to ringing on the last segment. Therefore, once the initial path of (C1 → T → C2) is established to have the minimum transit time of 6 ns, then we have immediately established the sequence of 10, 14, 18, 22 ns, etc. as valid times-of-pulse arrival. If we can establish *any* valid signal path that results in an even total transit between a pair of numbers in this first sequence, then we would have established pulse arriving times at *all* even values of t thereafter. This occurs for the path (C1 → T → C3 → T → C2),

which has a total transit time of 12 ns; thus, there will at least one set of reflections that will result in arriving pulses at t =12, 16, 20, 24, 28, 32 ns, etc. The final listing of times is the union of these two sequences.

(3) **The Death Star:**

	V_1	V_X	V_Y	V_1^+	V_1^-
State 0	0	0	0	0	0
State 1	12	0	0	12	0
State 2	24	6	0	15	9
State 3	24	10	-8	15	5
State 4	18	9	0	27/2	9/2
State 5	18	9/2	9/2	27/2	9