ECE 6361 Project 1: 5.8 GHz Signal Generator

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***Abstract*—This paper describes the design of a 5.8 GHz signal generator for use in a wireless power transmission system. An overview of the main components is given, and then design methods are provided so that the reader can reproduce the results. Simulated and measured results for various components are given where appropriate. Measured results of the overall system are provided with analysis of what did and did not work and why. The RF portion of the project operated as expected, however the PLL was unable to lock, impeding the frequency hopping algorithm written in the PIC. The final output was a single tone of 7 dBm.**

***Index Terms* — Frequency control, Microwave circuits, Microwave filter design, Microcontrollers, Phase locked loop, Power division, Wireless power transmission**

I. INTRODUCTION

The intention of this project was to create a 5.8 GHz transmitter for use in a wireless power transmission system. There is much interest in wireless power transmission for increasing the portability of personal electronics such as laptops, cell phones, and even home electronics. In keeping with the regulations necessary for commercial applications, the 5.8 GHz transmitter was designed to adhere to the FCC Part 15 guidelines for this unlicensed band.

A. FCC Part 15 Guidelines

The relevant portions of FCC Part 15 Guidelines are given below. Two specific rules are of the greatest importance. The first pertains to frequency hopping.

> Sec. 15.247(a)(1)(ii) "Frequency hopping systems operating in the 5725-5850 MHz band shall use at least 75 hopping frequencies. The maximum 20 dB bandwidth of the hopping channel is 1 MHz. The average time of occupancy on any frequency shall not be greater than 0.4 seconds within a 30 second period." [1]

The second rule speaks in regards to output power:

> Sec. 15.247(b)(1) "For … frequency hopping systems in the 5725-5850 MHz band: 1 watt [30 dBm]." [1]

Manuscript received July 22, 2009.

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On the most basic level, this design must provide a 75 channel frequency hopping algorithm; without remaining on any one channel for more than 0.4 seconds. Also, the maximum allowable output power of the system is 30 dBm. This restricts the output power of the signal generator to +7dBm, assuming that the intended power amplifier stage will provide an additional 23 dB of gain.

II. SYSTEM OVERVIEW

A. Components

1) Voltage Controlled Oscillator

The VCO used was a Mini-Circuits ROS-5776-119+ oscillator [2]. The notable features of this device are:

- Output frequency range: 5726-5826 MHz
- Tuning voltage range: 0.5-5V
- Output power: 1.5dBm (typical)

2) PLL Frequency Synthesizer

An Analog Devices ADF4107 frequency synthesizer, with external loop filter, was used along with the VCO to create the phase locked loop [3]. The PLL frequency synthesizer consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and programmable counters and dividers. The important features of the ADF4107 are the following:

- 2.7 to 3.3V supply power
- Programmable dual-modulus prescaler
- Programmable reference counter
- Programmable A and B counters
- 3-wire serial interface
- -5/+5 dBm sensitivity

3) Microcontroller

A Microchip Technology PIC18F4321 microcontroller was used to provide control to the ADF4107 PLL frequency synthesizer [4]. The important features of the MCU are:

- Internal oscillator (up to 8MHz)
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI interface
- Multiple interrupt sources
- 44 pin QFN package

4) Broadband RF Amplifier

Mini-Circuits GALI-39+ broadband RF amplifiers were used to boost the signal from the power divider output before sending to the output [5]. The important features of these devices are:

- Frequency range: DC to 7 GHz
- Output power: 10.5dBm (typical,1dB-comp.)
- Gain (at 5GHz): 16.1dB (typical)
- Max. operating current: 55mA

5) Quartz Oscillator

A 40 MHz quartz oscillator was used to provide a stable reference frequency input to the PLL. The device used was a Kyocera KC5032D series oscillator [6]. The features of this device are:

- Oscillation frequency: 40MHz
- Input Voltage: 5V

6) Power Divider

A Wilkinson power divider was designed to provide feedback from the VCO back into the PLL. It was designed to have equal (3dB) power split.

7) Band-pass Filter

A band-pass filter was used to ensure that no out of band signal reached the output of the system. For this purpose, a second order coupled line filter was designed. It was decided that second order should be used because the relatively high loss tangent of the FR-4 board ($\tan\delta = 0.02$), which created very high loss at 5.8GHz. In addition, because the output of the VCO was narrowband and could be controlled to a high degree by programming, it was determined that a second order filter should be sufficient. The intention was to keep the VCO output well within the specified frequency range, thus reducing the demands on the filter.

8) Circuit Board

The system was designed on a .062" FR-4 board ($\varepsilon_r = 4.7$, $\tan\delta = 0.02$). Advanced Circuits was the chosen manufacturer of the design. Features of the fabrication were 1 oz. Cu plate, green LPI solder mask, and top-side silkscreen for labels.

III. Design Methodology

A. PIC Programming

The following general strategy was employed to control the PLL to provide the desired functionality:

- Use SPI interface to load three 24-bit registers in the PLL frequency synthesizer[1]
- Interrupts via Timer 3 were used to time the frequency hopping
- Timer 3 was configured in 16-bit mode, and the timer was set to roll over every .32 seconds

The PIC microcontroller code was developed in the MPLAB® IDE, provided free from Microchip Technology Inc. The code was written in C and compiled using the Microchip C18 compiler.

[1] Counter Reset Method was used to program the PLL Frequency Synthesizer [3].

The following is a brief overview of the essential registers which were modified to implement the above strategy:

- OSCCON: use internal oscillator block at 4MHz ($F_{CPU}=F_{OSC}/4$)
- TRIS registers: set I/O pins as outputs
- T3CON: choose clock source (INTOSC), enable 16-bit operation
- TMR3L/H: set the time out period (16-bit)
- INTCON: [GIEH,GIEL] global/peripheral interrupt enable
- PIE2: [TMR3IE] enable interrupts from TMR3 rollover
- PIR2: [TMR3IF] Interrupt flag from TMR3 rollover
- PIR1: [SSPIF] MSSP Interrupt flag (used to verify end of byte write sequence)
- SSPCON1: Enable SPI function of MSSP and select correct polarity (rising/falling edge) for data transmission

Once configured, the SPI was very simple to use. Setting the SSPEN bit of the SSPCON1 register enabled the serial port (MSSP) and configured SCK (RC3) and SDO (RC5) as serial port pins. Then, simply loading a byte into the SSPBUF register enabled the write process.

The interrupts were enabled using the INTCON register as stated above. The Timer3 counter was then loaded (high byte first) to provide timer rollover in approx. 0.32 seconds. Finally, T3CON was used to enable the timer. The microcontroller code for the initialization is available upon request.

B. PLL Frequency Synthesizer

In order to program the PLL frequency synthesizer, three 24-bit registers were loaded with the correct bytes (MSB first). The correct values were obtained using the applet on Analog Devices website. As stated previously, we used the 'Counter Reset Method' to program the PLL. The three latches used here were:

- Reference counter latch
- N counter latch
- Function latch

The reference counter latch contains the 14-bit reference counter [bits 15:2]. The N-counter latch contains the 13-bit B counter [bits 20:8] and the 6-bit A counter [bits 7:2]. Finally, the function latch contains the prescaler value [bits 23:22], the phase detector polarity bit [bit 7], and the counter reset bit [bit 2]. It should be noted that the last 2 bits of the 24-bit transmission select which latch will be loaded. The division ratio (N) for the PLL is derived from the following formula:

$$N = BP + A \quad (1)$$

The VCO output frequency can be derived from the following formula:

$$f_{VCO} = [(P \times B) + A] \times \frac{f_{REFIN}}{R} \quad (2)$$

where f_{VCO} is the output frequency of the VCO, f_{REFIN} is the reference frequency input from the quartz oscillator, R is the reference counter value, and P, B, and A are the respective counters.

The PLL chip is programmed by writing to the function latch, then to the R counter latch, then to the N latch, then to the function latch again. The first write to the function latch contains a'1' in bit 2. This holds the counters on reset until the R, A, and B counters are loaded. The second write to the function latch clears this bit, enabling the counters. Note that writing to a given latch requires bringing the LE bit of the PLL chip low, writing 3 bytes to a given register, and then bringing the line high again.

In order to change frequency, only the A and B registers [located in the N latch, see datasheet] on the PLL need to be modified. The prescaler (set to 32 for this application), will not change, as it only serves to divide down the RF input frequency from the VCO to a manageable frequency for the PFD. Likewise, the reference counter (R latch) is used to divide the reference frequency in from the crystal oscillator to 1 MHz, the resolution frequency required for the application. In the frequency hopping algorithm, the A and B counters are just incremented, as evidenced by equation 2 above.

C. *Power Divider*

The simplest form of an equal power split Wilkinson power divider is shown in Fig. 1 [7]. The structure of an equal split Wilkinson power divider consists of 2 arms (each quarter-wave transformers) of impedance 1.414xZo with a 100 ohm resistor connecting each arm.

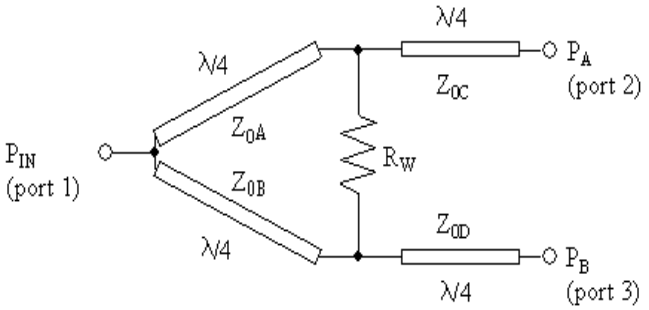


Fig. 1. Topology for the equal-split Wilkinson power divider.

When a signal enters port 1, it splits into equal-amplitude, equal-phase output signals at port 2 and 3. There is no current flow through the 100Ω resistor, so the two output ports are terminated with 50 ohm resistances. Initial design values for the power divider are shown in Table I.

TABLE I
INITIAL CHARACTERISTIC IMPEDANCES OF THE WILKINSON DIVIDER

Parameter	Value
Z0A	70.7 Ω
Z0B	70.7 Ω
Z0C	50 Ω
Z0D	50 Ω
Rw	100 Ω

Once the hand calculated values were obtained, the power divider was designed and simulated using Agilent ADS. The goal was to obtain -3 dB loss for S13 and S12, while keeping S23 isolation, and providing return loss as low as possible. Fig. 2 shows the schematic of the initial power divider, and Fig. 3 shows the simulated results for the S-parameters of the circuit.

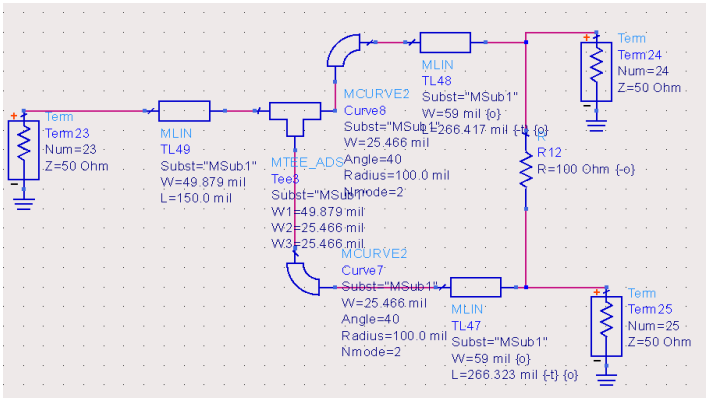


Fig. 2. Initial power divider schematic.

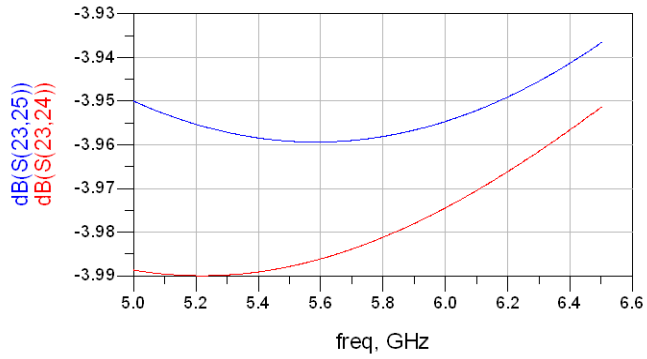


Fig. 3. Hand calculated simulation results.

As shown in Fig. 3, the actual divider between the two ports, 2 and 3, was -3.95 dB and -3.99 dB rather than 3dB. Also, isolation between ports 2 and 3 [S23], turned out to be -13 dB which is not excellent, but it is acceptable. The return loss was -6.8 dB, which was determined to be unacceptable (desired less than -10dB). Using the tuning feature of ADS, the parameters were tweaked and the design was improved to meet specs, as shown in the figure 5 below.

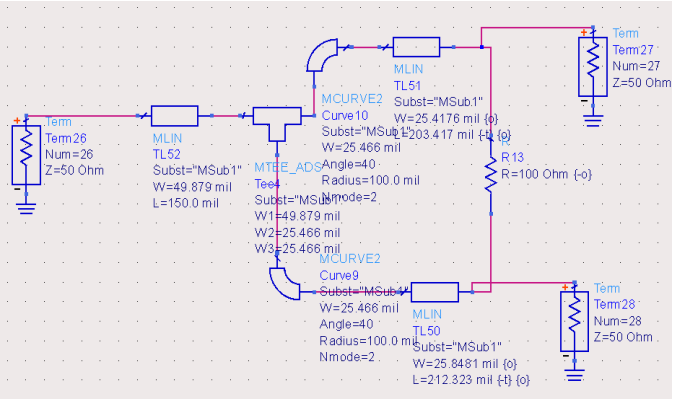


Fig. 4. Wilkinson power divider after tuning.

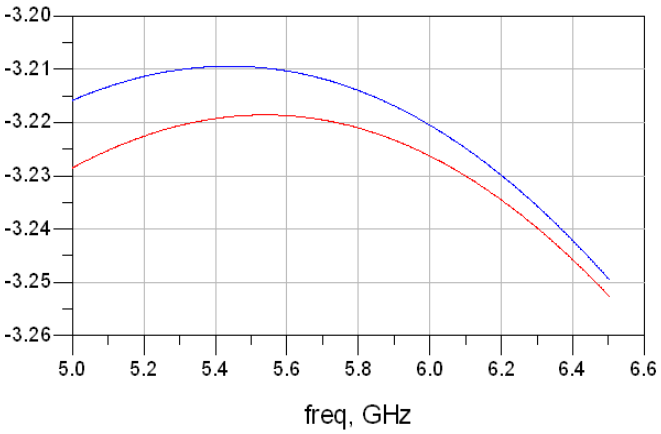


Fig. 5. Simulation results after tuning.

After tuning the power divider design in ADS, the results were not at optimum (-3 dB); however, they were much better than the original hand calculated design. The original design was much further away from 3 dB, and the difference in power split from the two ports in the original design was greater as compared to the tuned design. The following table summarizes the differences and improvements between the two designs. The overall final simulation results are shown in Fig. 6 and a comparison is given in Table II.

TABLE II
DIFFERENCES BETWEEN THE INITIAL AND FINAL DIVIDER DESIGNS

Parameter	Original design	Tuned Design
Return Loss (S11)	-6.8 dB	-38 dB
Isolation (S23)	-13 dB	-42 dB
S12	-3.981 dB	-3.221 dB
S13	-3.958 dB	-3.214 dB

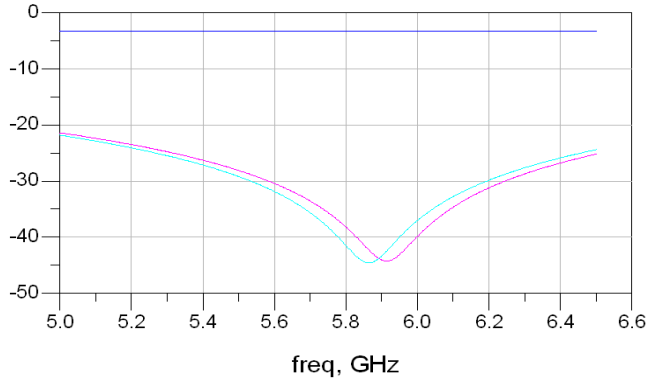


Fig. 6. Final simulation results

D. Bandpass Filter

1) Design Specs

The desired specifications for the band-pass filter (BPF) were

- Center frequency, f_o = 5.7875 GHz
- Bandwidth D = 125 MHz

A coupled line design was used. This method was chosen due to0 the ease of fabrication using microstrip topology, and for its effectiveness with bandwidths less than 20% [7]. A Chebyshev filter response was used because it provided the sharpest cutoff of all the filter functions (excluding Elliptic and Quasi-elliptic responses, which are much more difficult to design and implement). Since matching at both ports was desired, it was necessary for *N* to be odd and greater than 1. The *N* that provided the best performance (met minimum trace width of 10 mils, and provide sharpest response) was *N* = 5. The even and odd mode equations were used to determine the characteristic impedances of the coupled sections (where the g_k terms are the filter prototype values for a 5th order Chebyshev band-pass filter). Table III shows the results for the design.

$$Z_o J_1 = \sqrt{\frac{\pi D}{2 g_1}} \tag{0.1}$$

$$Z_o J_n = \frac{\pi D}{2\sqrt{g_{n-1} g_n}}, n = 2,3 \tag{0.2}$$

$$Z_o J_{N+1} = \sqrt{\frac{\pi D}{2 g_N g_{N+1}}} \tag{0.3}$$

$$Z_{oe} = Z_o \left[1 + JZ_o + (JZ_o)^2\right] \tag{0.4}$$

$$Z_{oo} = Z_o \left[1 - JZ_o + (JZ_o)^2\right] \tag{0.5}$$

TABLE III
COEFFICIENTS FOR THE BAND-PASS FILTER DESIGN

N	g_n	Z_J	Z_{oe}	Z_{oo}	C_DB
1	1.7058	0.16616762	59.688964	43.0722	-8.27301
2	1.2296	0.032521826	51.678974	48.42679	-23.4582
3	2.5408	0.026647332	51.367870	48.70314	-25.2381
4	1.2296	0.026647332	51.367870	48.70314	-25.2381
5	1.7058	0.032521826	51.678974	48.42679	-23.4582
6	1	0.036062585	51.868154	48.2619	-22.531

2) Simulation and Optimization

The ADS simulation schematic of the initial band-pass filter design is given in Fig. 7, followed by simulation results in Fig. 8. Changes in microstrip line width are accounted for by MSTEP, and the coupled line sections are modeled by MCLIN.

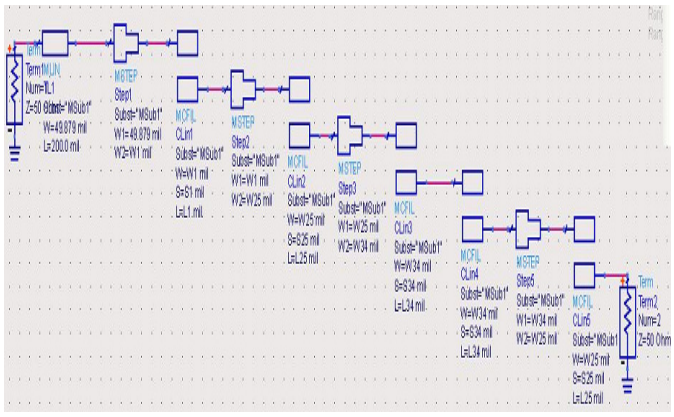


Fig. 7. ADS schematic of coupled-line BPF.

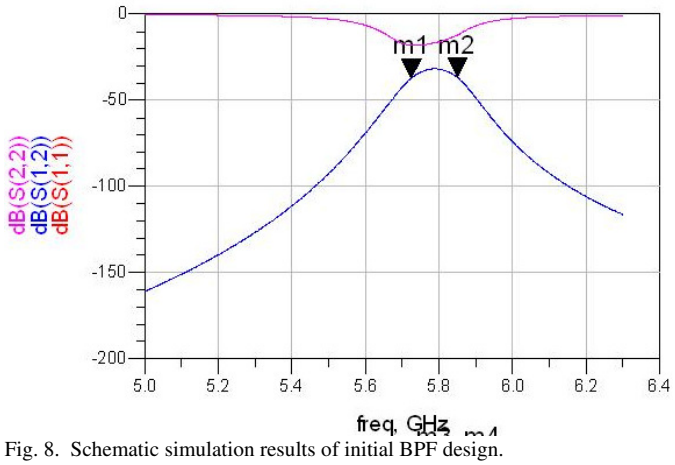


Fig. 8. Schematic simulation results of initial BPF design.

Initial simulation results were very far from the expected results. The pass-band attenuation and the return loss were very high. A lower order filter was used in the updated design, as it was determined that one of the main reasons for high attenuation was the excess number of stages (due to very high loss tangent of FR-4 substrate used in the design).

A 2nd order filter was designed to compensate for the high loss-tangent attenuation. The new design is shown in Fig. 9 and the resulting simulation is shown in Fig. 10.

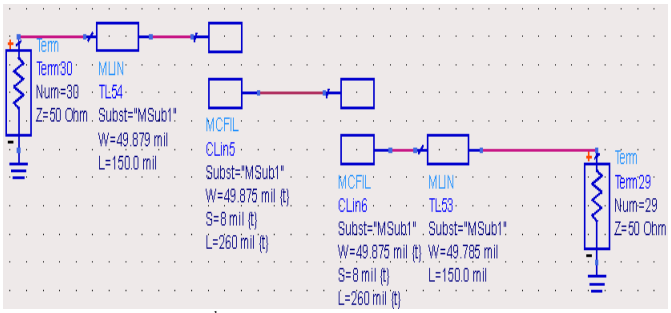


Fig. 9. Schematic for 2nd order BPF design.

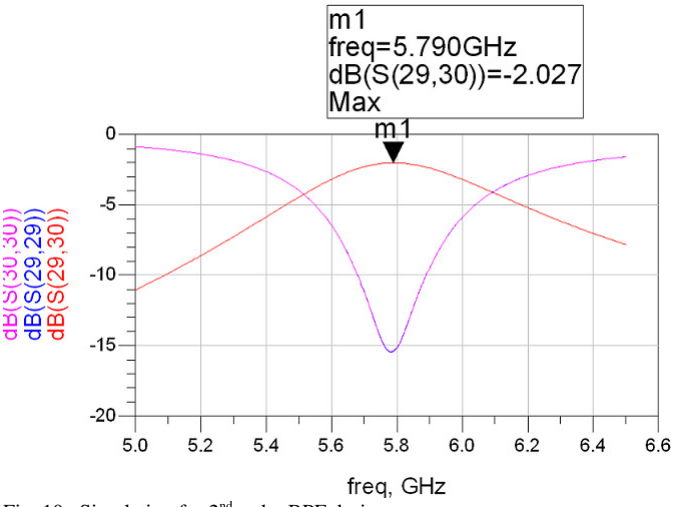


Fig. 10. Simulation for 2nd order BPF design.

The trade-off between bandwidth and stop-band attenuation was used while designing the second BPF. Finally, the 2nd order filter was chosen for use in the final design.

E. Radio Frequency Amplifier

One of the most important characteristics of an amplifier is linearity. That is, the ability of the stage to amplify all the parts by the same amount so that all the signals are amplified equally. In this project, the Mini-Circuits RF Amp Gali-39+ is used. It is rated to work up to 7 GHz. The S-parameters were obtained from Mini-Circuits and simulated in Agilent ADS. The bias circuit was designed according to the datasheet for the RF Amp. The RF choke, capacitor, and 107Ω resistor were used to have 3.3VDC voltage at each amplifier to set the proper bias current. Fig. 11 shows the schematic for the RF amplifier along with biasing circuitry.

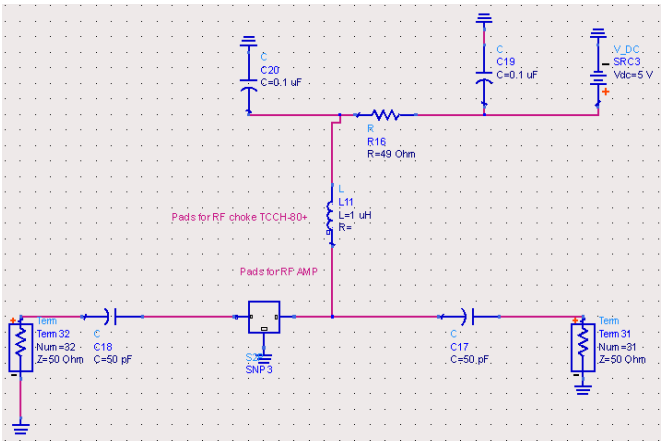


Fig. 11. Schematic for RF Amp with the bias network.

The simulation results are shown in Fig. 12.

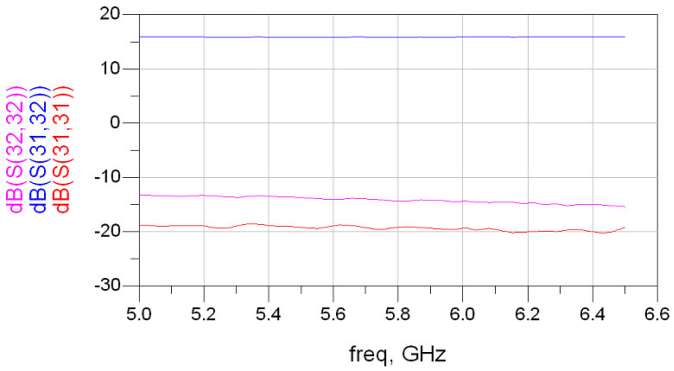


Fig. 12. S-parameter simulation for the RF Amp design.

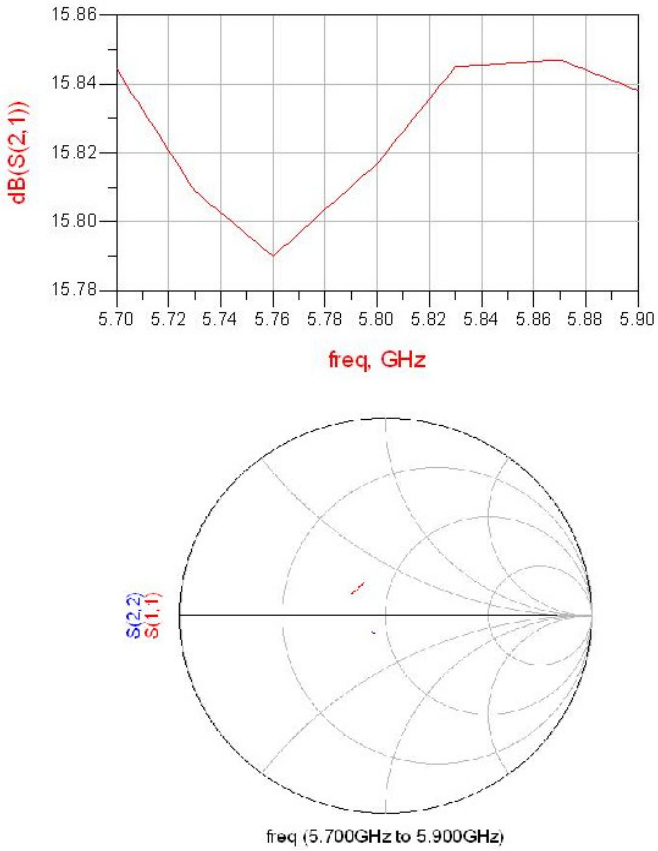


Fig. 13. Gain and matching for the RF amplifier.

As shown in the above simulations, the gain is over 15 dB, and the return loss was below -15 dB. The Smith Chart shows the matching is very close to 50 Ω for the RF Amp, and hence no extra matching network was required. Thus, the amplifier with suggested bias network is used as the final design.

F. Printed Circuit Board

Three priorities were central in the design of the printed circuit board: size, isolation, and ease-of-use. The high loss tangent of FR-4 at 5.8 GHz made a short RF signal path absolutely necessary. The sensitivity of the components required the absence of interference. Unfortunately, these two goals are often in opposition.

Part placement led to the small size of the board. First, passive components were placed as close as possible to the active circuits utilizing them. This can be observed throughout the board in Fig. 14 and in a larger version, Appendix A (schematic is in Appendix B). For example, the choke, resistors and capacitors for the RF amplifiers are all located directly above the amplifiers themselves. Second, no unnecessary length was added to the RF path. The positions of the PLL and the VCO were based solely on the smallest reasonable size of the power divider. On the other side of the divider, traces were kept only long enough to ensure soldering would not be difficult. The distance from the divider to the output connector was only 2.5 inches.

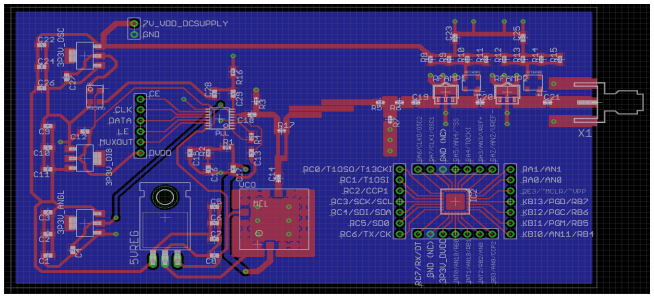


Fig. 14. PCB Layout of the final design.

Supply isolation was broken up into four sections: Analog 3.3 V, Analog 5 V, Digital, and Oscillator. A different voltage regulator was intended to supply each section, but the crystal oscillator's enable voltage was supplied by the Oscillator voltage regulator, while its V_{DD} was supplied by the Digital voltage regulator. Otherwise the regulators separated the V_{DD} for each section.

Spatial isolation was used as much as possible between the low and high frequency portions of the board. This can be seen by the open areas on the right side of the PCB where the RF signal traces have much more room. Also, the PIC processor's headers supplemented the already large spatial isolation from the RF.

To optimize ease-of-use, the board was designed to only need one external supply, and all the PIC and PLL communication pins were placed on headers. The large operating range of the voltage regulators and RF amplifiers made it possible to use a single 7 V supply for the entire board. The regulators transformed the voltage to their specified output, and the resistors for the RF amplifiers were chosen to match the nominal current for 7 V.

Pulling all the PIC pins and the communication pins for the PLL allowed on-board programming and the flexibility to use any output pins on the PIC. Short jumper wires could be used to connect the two sets of headers in any orientation needed. It also made it possible to debug the PLL using any off-board PIC. The ability to isolate a specific part was extremely valuable.

There were other miscellaneous design decisions that impacted that final version of the PCB. A bottom layer ground plane was implemented. In only two instances was layer used for signal routing. Next, because vias can often be seen as inductors, whenever possible, multiple vias are used in parallel for a ground connection. Any inductance seen looking into these vias was effectively reduced. Also, for exceptional grounding of the VCO, a small, top layer ground plane was used in tandem with multiple vias to the bottom ground plane. This method was helpful in obtaining a clean tone output. Last, four resistors were used in parallel for the biasing of each RF amplifier. Surface mount resistors often have a power tolerance as low as one-eighth of a Watt, so using the parallel combination ensured no resistor would exceed its power limit.

The final Bill of Materials is listed in Appendix C.

IV. Results

A. Successful Sections of Project

1) RF circuitry

The RF circuitry of the board was tested and verified independently from the low frequency mixed signal portions. This was done to verify the operation and stability of the RF amplifiers and the proper operation of the power divider and band-pass filter. The results are shown in Fig. 15 below.

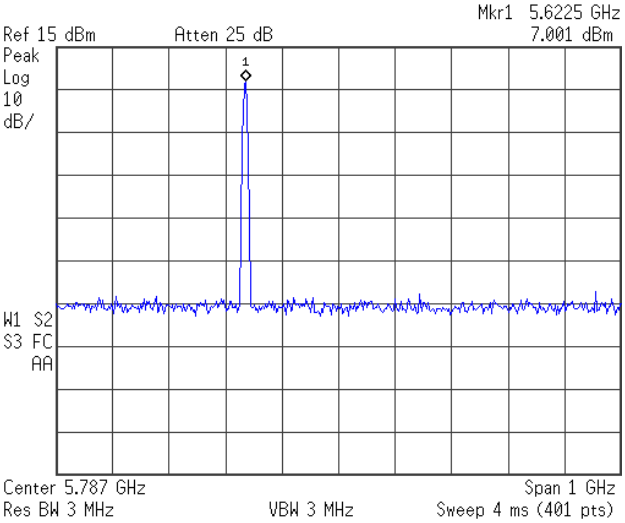


Fig. 15. Spectral output of system.

It was noted that the power output of the system was +7dBm, which met the specified design requirement for power output.

2) PIC Microcontroller

a) SPI Interface

The output of the PIC microcontroller was verified using an oscilloscope. Channel 1 was connected to the serial clock line, and channel 2 was connected to the serial data line. The scope capture is given in Fig. 16 below.

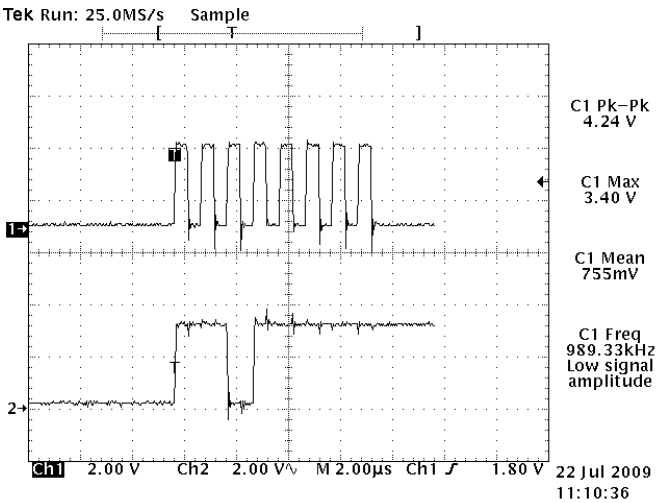


Fig. 16. Screen capture of SPI operation (SCK top, SDK bottom).

The traces were positioned over one another and the bits were recorded. After translating back into HEX, it was verified that the data was correct. Note that here the frequency hopping algorithm was disabled so that one constant 24 bit sequence could be observed for validation purposes.

b) Timing via Interrupts

The functioning of the interrupts was also verified using an oscilloscope. To do this, the RB0 pin was toggled inside the interrupt service routing and the scope was connected to RB0 to verify the timing. The result is shown in Fig. 17 below.

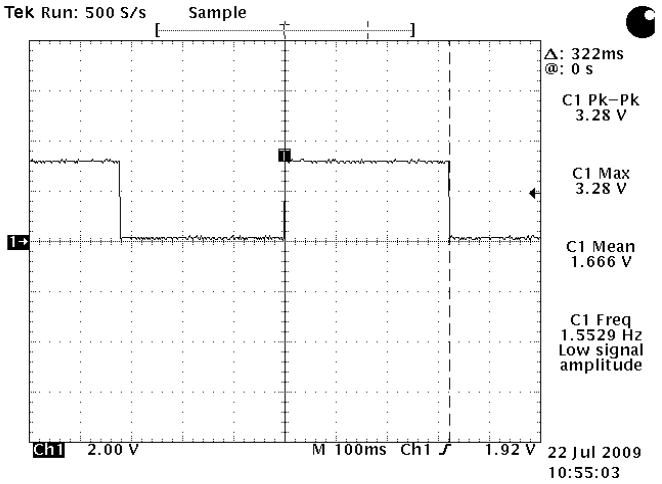


Fig. 17. RC3 pin showing interrupt timing.

Note that the period between bit toggles is 0.32 seconds (we chose this value to ensure compliance), corresponding to roughly 32K (plus extra time for other minor code executions) clock cycles of the timer (f_{timer} = 1MHz).

c) Programming of the PLL Chip

The programming of the PLL chip was verified using the MUXOUT function of the chip. This function provides access to various internal points of the PLL chip. By programming bits 6:4 of the function latch, it is possible to choose one of 8 points inside the chip. The easiest way to verify operation is using the digital V_{dd}. If this option is chosen, initially the MUXOUT will be floating between 0 and DV_{DD}. If the PLL chip is programmed correctly, the MUXOUT will immediately change to DV_{dd} (3.3V). This was observed on the oscilloscope as shown in Fig. 18 below.

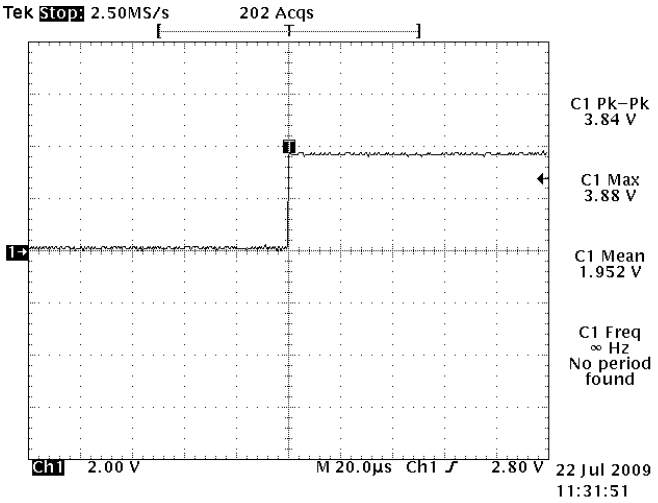


Fig. 18. MUXOUT of PLL chip showing DVdd.

B. Problematic Parts of Project

Although we were able to program the PLL, as verified above, we were not able to get the PLL to lock. This was evident on the spectrum analyzer, where the output of the system was always either the minimum or maximum possible frequency for the VCO. It was also verified by the analog voltage out from the PLL chip, which was always one of the two extremes for the tuning voltage, implying a free running VCO.

The functioning of the VCO itself was tested by directly connecting an analog input from a lab power supply and adjusting the voltage. This produced the desired frequency shift, proving the correct operation of the VCO.

C. Lessons Learned and Explanations

After the testing of the final design, two major lessons were learned. First, more isolation of the PLL loop filter and RF signal path was needed. Cross-talk between these traces could have been a major factor in the PLL not being able to lock on any specific frequency. Second, even more header pins would have been better. As mentioned earlier, isolating specific parts is quite valuable during the debug phase of testing. For example, having a backup pin on the output of a voltage regulator would be a suitable replacement if that regulator failed.

One possible explanation for the inability of the PLL to lock is the coupling of the VCO output to the PLL Ref in. Due to cost constraints, we did not separate the ground for the RF and the lower frequency components. Therefore, it is possible that the VCO was bleeding through into the low frequency sections of the system and interfering with the phase measurements for the PLL frequency phase detector.

Another possible explanation for the inability to lock the PLL comes from the chip itself. As per the datasheet, the minimum input power to the PLL chip must be -5 dBm. Even with a perfect (3 dB) power divider and assuming no system losses in the microstip lines, the power input to the PLL chip would be -3dBm (VCO output power is 0dBm). We know that the loss tangent of the FR-4 board is high, so the loss here

will be in addition to the loss in the power divider. Possibly the input power to the PLL chip was below the sensitivity level. Several solutions exist to remedy this problem. We could have chosen a chip with higher sensitivity (lower required input power, or we could have designed an unequal split Wilkinson power divider. However, this option would have required extra matching networks, increasing the size and complexity of the design and adding additional loss. Finally, we could simply place an amplifier between the output of the power divider and the input to the PLL chip to boost the signal. The latter suggestion would be preferable.

REFERENCES

[1] FCC Part 15 Regulations, February 16, 2006

[2] Mini-Circuits ROS-5776-119+ datasheet. Available: http://www.propagation.gatech.edu/ECE6361/resources/ABM10_Quartz_Oscillator.pdf

[3] Analog Devices ADF4107 datasheet. Available: http://www.propagation.gatech.edu/ECE6361/resources/ADF4107_PLL_Frequency_Synthesizer.pdf

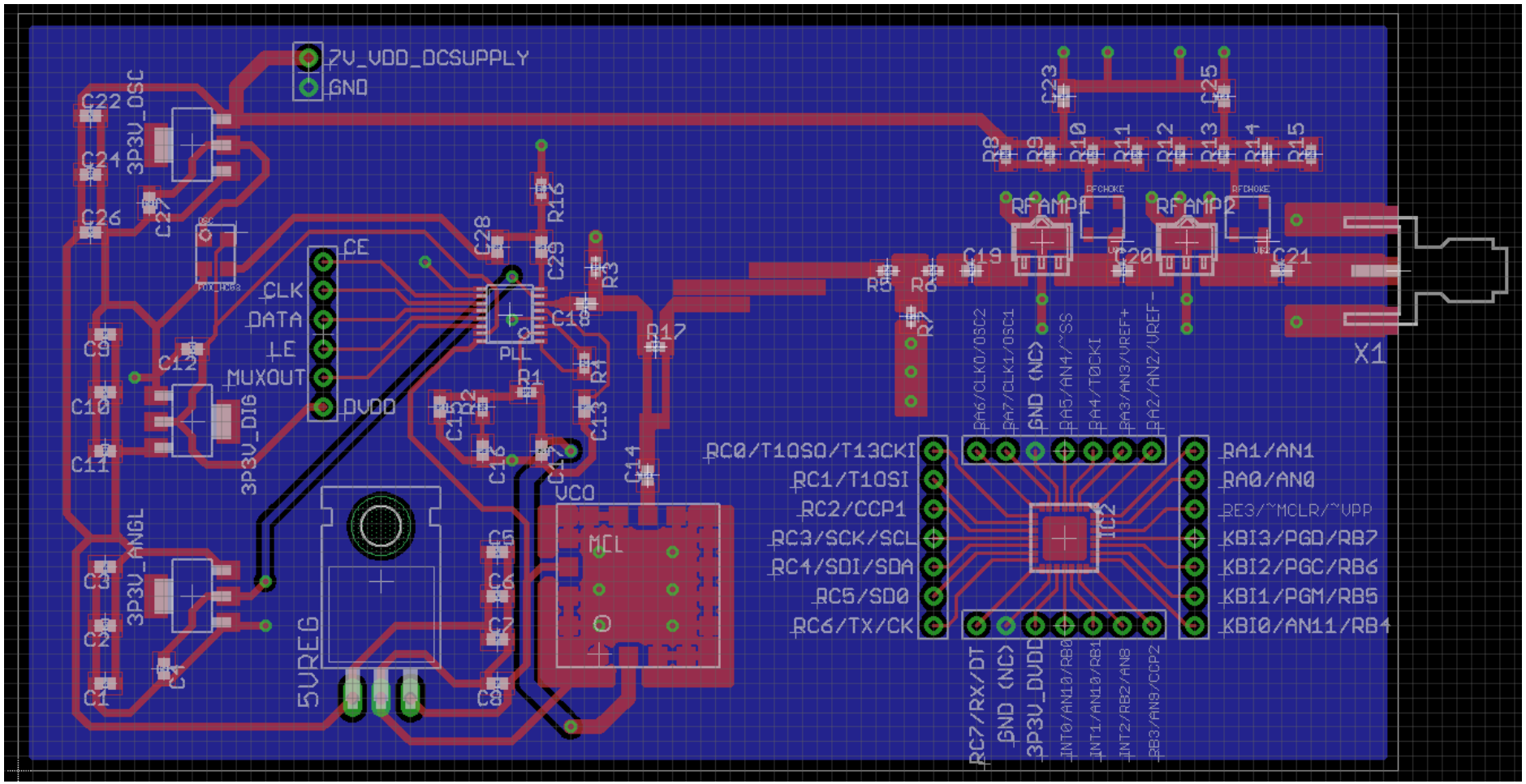
[4] Microchip PIC18F4321 datasheet. Available: http://ww1.microchip.com/downloads/en/DeviceDoc/39689E.pdf

[5] Mini-Circuits Gali-39+ datasheet. Available: http://www.propagation.gatech.edu/ECE6361/resources/Minicircuits_Broadband_RF_Amp.pdf

[6] Kyocera KC5032D datasheet. Available: http://global.kyocera.com/prdct/electro/pdf/clock/131_e.pdf

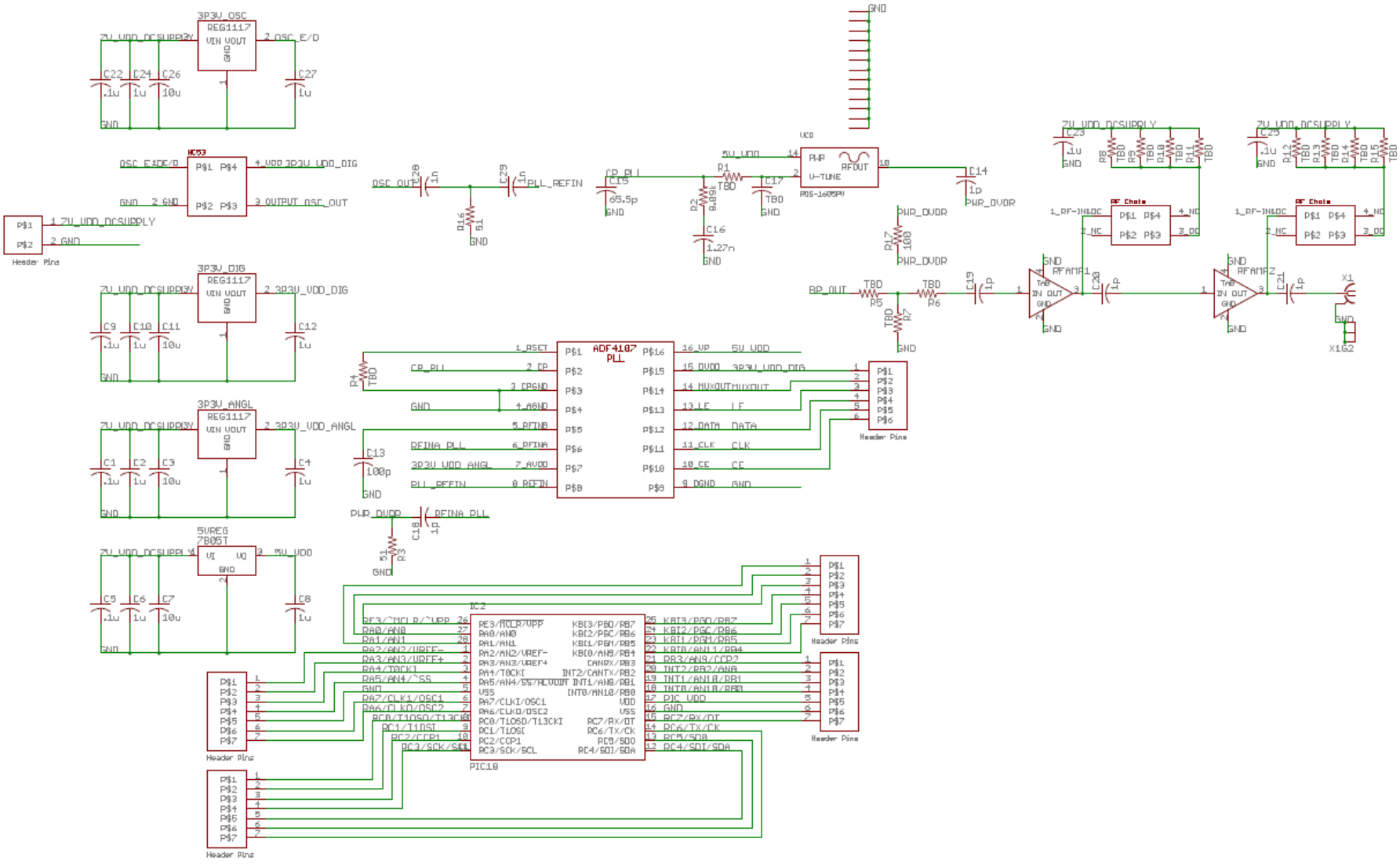
[7] D. M. Pozar, “Microwave Filters,” in *Microwave Engineering*, 3rd ed. Hoboken: John Wiley, 2005.

Appendix A: PCB Layout


7V_VDD_DCSUPPLY
GND
3P3V_OSC
3P3V_ANGL
3P3V_DIG
5VREG
CE
CLK
DATA
LE
MUXOUT
DVDD
PLL
VCO
MCL
RFAMP1
RFAMP2
RFCHOKE
X1
IC2
RC0/T1OSO/T13CKI
RC1/T1OSI
RC2/CCP1
RC3/SCK/SCL
RC4/SDI/SDA
RC5/SDO
RC6/TX/CK
RC7/RX/DT
GND (NC)
3P3V_DVDD
RA6/CLKO/OSC2
RA7/CLK1/OSC1
GND (NC)
RA5/AN4/~SS
RA4/T0CKI
RA3/AN3/VREF+
RA2/AN2/VREF-
RA1/AN1
RA0/AN0
RE3/~MCLR/~VPP
KBI3/PGD/RB7
KBI2/PGC/RB6
KBI1/PGM/RB5
KBI0/AN11/RB4
INT0/AN10/RB0
INT1/AN10/RB1
INT2/RB2/AN8
RB3/AN9/CCP2

Appendix B: PCB Schematic

Can be provided in a separate, higher-quality document.



Appendix C: Bill of Materials

ECE 6361 Project 1 Bill of Materials						
Part Description	Manufacturer	Part Number	Cost (USD)	Quantity Needed	Line Total (USD)	Comment
Voltage Controlled Oscillator	Mini-Circuits	ROS-5776-119+	29.95	1	29.95	
Phase-Locked Loop	Analog Devices	ADF4107	2.67	1	2.67	
PIC Microcontroller	Microchip	PIC18F4321	3.41	1	3.41	
Broadband RF Amplifier	Mini-Circuits	GALI-39+	1.19	2	2.38	
Quartz Oscillator	Kyocera	KC5032D	1.64	1	1.64	Cost of comparable component from Digi-Key.
3.3 V Regulator	Diodes Inc	AP1117E33G-13	0.77	3	2.31	
5 V Regulator	Fairchild Semiconductor	LM7805CT	0.45	1	0.45	
RF Choke	Mini-Circuits	TCCH-80	3.45	2	6.9	
Surface Mount Rs and Cs	Various	Various	0.33	44	14.52	Because so many different parts are needed, and tuning from board to board may vary, this line is only approximate.
Male Pin Headers	Samtec Inc	TSW-150-07-T-D	4.1	1	4.1	
SMA Jack	Molex Connector Corporation	73251-1150	3.69	1	3.69	
Board Fabrication	Advanced Circuits	N/A	33	1	33	This is not a specific component but is still a part of the total cost.
				Total Cost	105.02	