5.8 GHz Power Amplifier Design

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***Abstract* -This paper gives a step-by-step account of the design, assembly and testing of a Power Amplifier operating from 5.7 to 5.9 GHz. The design of Class A Power amplifier was performed in Agilent ADS and the performance was tested with Nitronex NPTB0004 HFET.**

***Index Terms*—RF Power Amplifier, HFET**

Introduction

The wireless communications market places ever increasing demands on emerging systems designs. A critical element in Radio Frequency (RF) front ends is the Power Amplifier (PA). Critical specifications for PA design include linearity and efficiency. Linearity must be maximized in order to reduce signal distortion and minimize Adjacent Channel Leakage Ratio (ACLR). This paper describes the process of designing a single stage PA for operation in the 5.7-5.9 GHz band.

The active device specified for this design was a Nitronex NPTB0004 GaN HFET. The circuit was to be fabricated on evaluation board using passive elements available from the Georgia Tech ECE department. Table I shows the performance specifications for the designed Power amplifier.

Device Modeling

The model provided by Nitronex was used as a starting point for the amplifier design. The load pull and source pull simulations were performed in ADS to determine the optimal load and source impedance. There was a stark contrast in the impedance versus frequency characteristics of the device before and after load/source pull optimization. The optimized load and source impedance are listed in Table II.

The device was biased with Vdd of 24 V and gate bias of -1.4 V to set Drain current of 50 mA. The I-V characteristics of the device and the choice of gate bias point are shown in the Figures 1 and 2. At 50 mA drain current the transition frequency of this device is 6.6 GHz which sets the upper limit on the frequency of operation of this device.

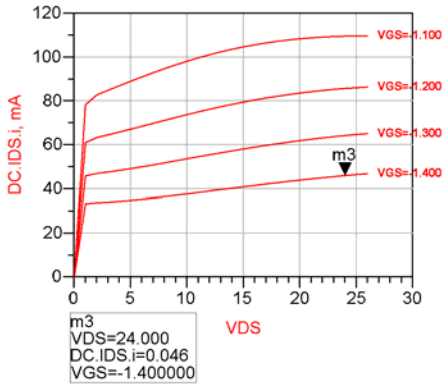

Figure 1 - Device I-V Characteristics

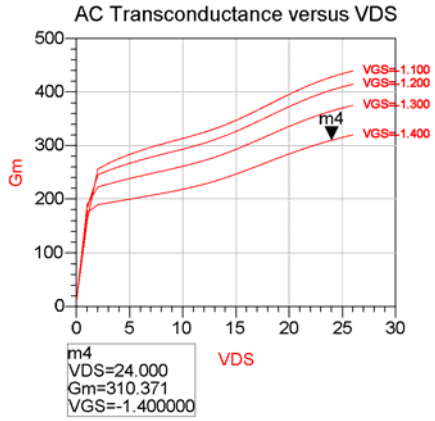

Figure 2 – AC Transconductance vs Vds

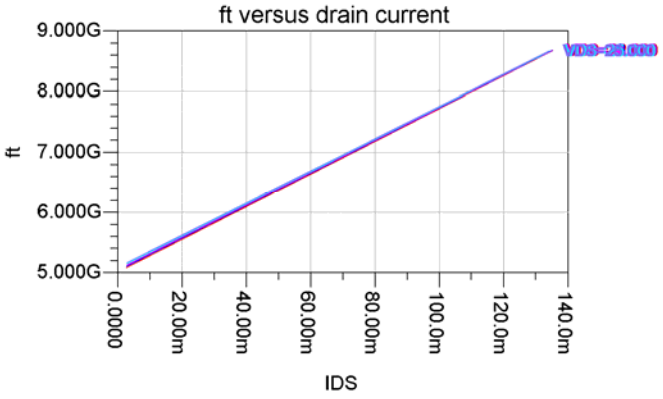

Figure 3 – Transition Frequency vs Drain Current.

TABLE I

PERFORMANCE SPECIFICATIONS

Parameter	Symbol	Specification
Input/Output Impedance	Z_0	50Ω
Drain DC Supply	V_{DD}	24 V
Gate DC Supply	V_{GG}	-1.4 V
Frequency Range	f_0	5.7 - 5.9 GHz
Gate DC Supply Current	I_G	≤ 6mA
Input Return Loss	$\|S_{11}\|$	≤ -12 dB
Small Signal Gain	G	≥ 10 dB @ 2 GHz > -12 dB @ 5.7 GHz
Stability	K	>1

TABLE II

$Z_{L\text{-}OPT}$ SIMULATED VS. Z_S MEASURED

Frequency	From Model	Final Design
5.7 GHz	13.75-j*15.80 Ω	15.2-j*16.3 Ω
5.8 GHz	10.02-j*17.85 Ω	13.65-j*14.1 Ω
5.9 GHz	9.61-j*21.50 Ω	11.5-j*12.05 Ω

$Z_{S\text{-}OPT}$ SIMULATED VS. Z_S MEASURED

Frequency	From Model	Final Design
5.7 GHz	13.75-j*15.80 Ω	15.2-j*16.3 Ω
5.8 GHz	10.02-j*17.85 Ω	13.65-j*14.1 Ω
5.9 GHz	9.61-j*21.50 Ω	11.5-j*12.05 Ω

Matching Network Design

Bias Networks

The bias networks were designed to present high impedance to the RF signal at the gate and drain by using inductors. The inductor values are chosen such that their resonant frequency are at 5.8 GHz. Decoupling capacitors of the order 10 uF, 1uF and 0.1 uF were used to eliminate DC bias ripple as well as dissipate RF energy. The gate bias voltage of -1.4 V had ripple in the order of 300 mV which requires decoupling capacitors to eliminate this problem.

Input Matching Network

The first set of measurements were taken for S_{11} with the device mounted on the board and biased, but without matching networks. These measurements were de-embedded in ADS to obtain the input impedance at the device terminal. In order to ensure unconditional stability (Figure 4) from 0.5-6GHz, a 20Ω series resistor was used at the gate of the transistor. The circuit was then conjugate matched from this point to the 50Ω impedance presented by the trace line.

The input matching network shown in Figure 5, was designed using the Smith Chart utility in ADS. The input matching network uses a series transmission line and shunt capacitor. A series capacitor in the order of 100 pF is placed as DC blocking capacitor. A lumped component matching at 5.8 GHz is a viable option but it would not provide the option of tuning. Transmission line with a shunt capacitor allowed us to tune the matching until the best possible performance of S11 was obtained.

Output Matching Network

To design the output matching network, S_{22} of the biased, unmatched system was measured and de-embedded back to the device terminals. Simulations were then performed to determine the impedance presented to the drain that would maximize small signal gain. The matching network was designed in the same fashion as the input matching network. The matching was designed with a wideband characteristic to ensure it covered the required frequency band.

This method gave several different optimal load impedances, indicating that trade-offs would be necessary to meet all specifications. Since these points all fell in the lower left quadrant of the Smith chart, an output matching network using shunt capacitors and series transmission line was chosen based upon the same mentality in choosing the input matching network topology. The output matching network can be seen in Figure 5.

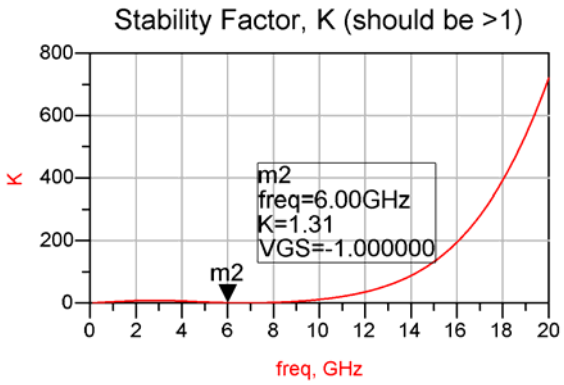

Figure 4 – Stability Factor versus Frequency characteristics.

Implementation

Power handling capability was ensured through the use of capacitors with 50V breakdown ratings, as well as the use of a larger form factor inductor with a 1000mA current handling capability on the drain biasing network, well above the maximum swing.

There were several non-idealities that necessitated the "tweaking" of the system. First, the package size of the 0603 capacitors used was relatively large compared to the wavelengths of interest, making the precise placement of capacitors along transmission lines difficult. In addition, because of component tolerances, several capacitors of the same nominal value often gave slightly different results when installed in the circuit, leading to a trial-and-error approach. When adjusting the matching networks, it was found that altering the output matching network impacted the measured S_{11}, showing that our transistor could not be approximated as a

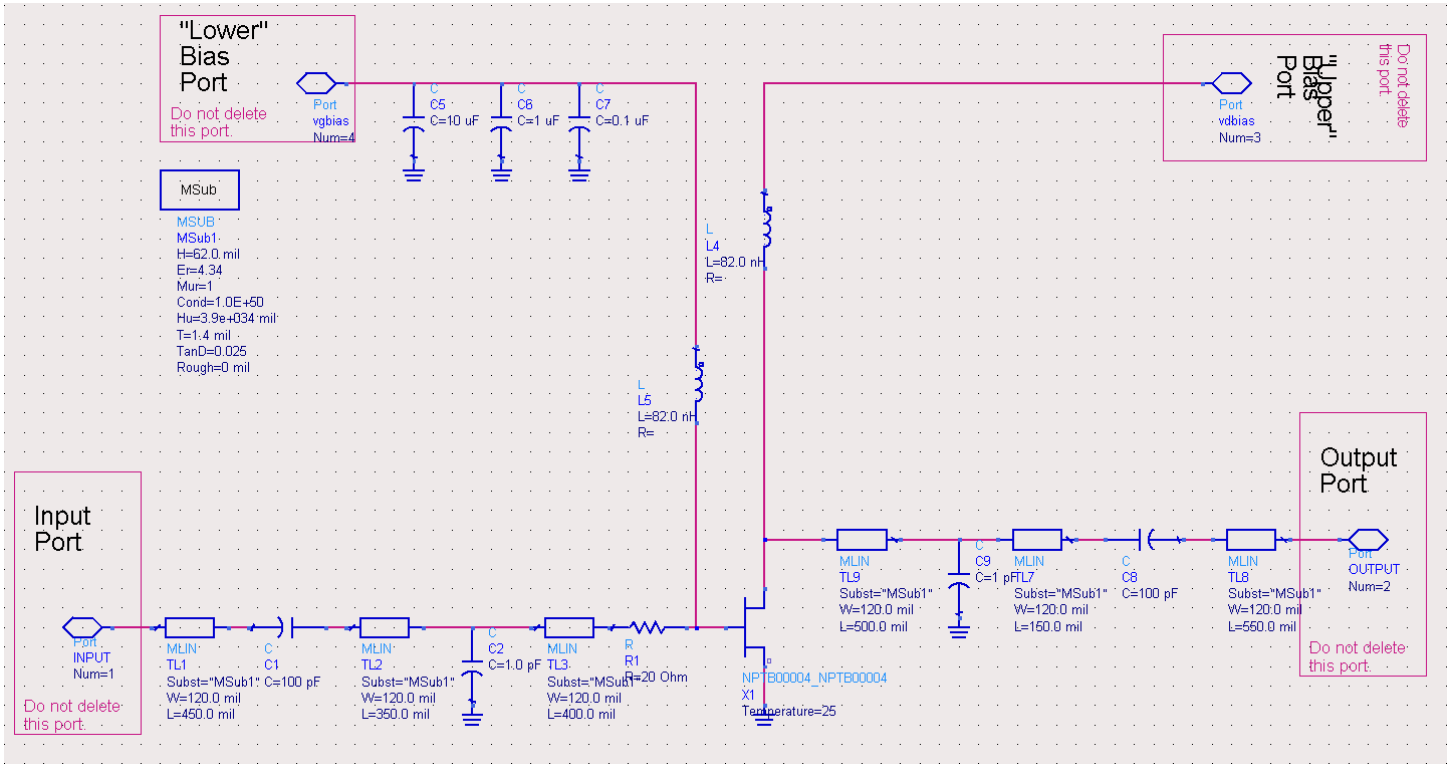

Figure 5 – Schematic of the Power Amplifier with Bias networks, Input and output matching networks.

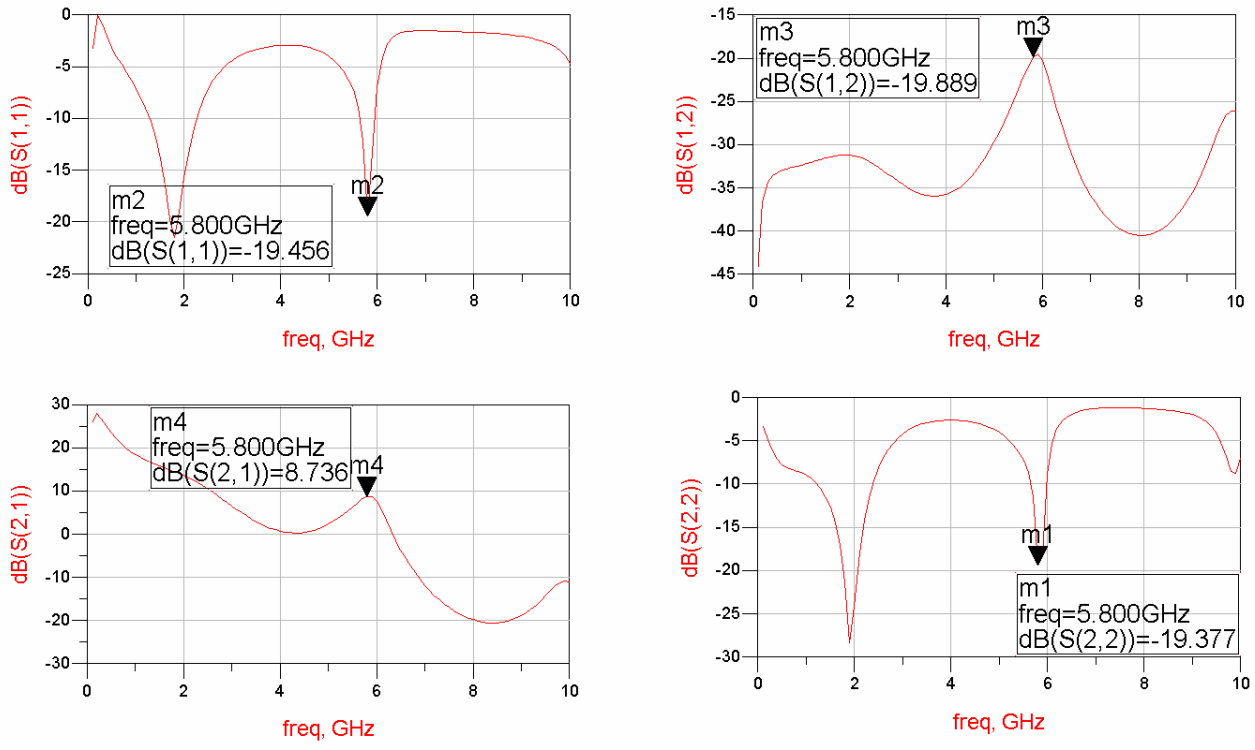

Figure 6 – Large Signal S Parameter Simulations for Power Amplifier with proper matching networks.

unilateral device at this bias point. This added an additional tradeoff in that altering the output match to increase gain worsened the input match. However, it was decided that the gain and saturation levels were more important for a power amplifier than a slight improvement in reflection coefficient on the input.

Bias Point

After designing the input and output matching networks, the amplifier was tested with several bias points. It was found that increasing the quiescent drain current from 50 mA to 100 mA had several effects. The higher bias current increased the small signal gain. Increase in gain would improve the linearity performance and intermodulation performance, but hurts the reverse isolation performance. The input power applied to the device is about 30 dBm which generates an output power of 37 dBm in simulation, since the Output saturation power is 37 dBm. The gain expected at 5.8 GHz is about 8 dBm as per simulation results.

Thermal Analysis

The maximum junction temperature was calculated using the thermal equivalent circuit shown in Figure 6. The DC power consumption was 1.2 W at 5.8 GHz. The junction-pin thermal resistance was taken to be 41 °C/W from the NPTB0004 datasheet and the thermal resistance of the board was calculated using (1) for a solder-filled via.

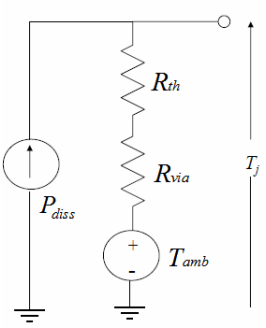

Figure 7 – Junction Thermal Equivalent Circuit

$$R_{via} = \frac{h}{\sigma \times \pi \times (R_{outer}^2 - R_{inner}^2) \times N_{via}} \quad (1)$$

Each via hole is 62 mils long with a radius of 10 mils and was calculated to have a thermal resistance of 97.12 °C/W. The 50 vias thermally connected in parallel to the source pad gave a total via thermal resistance of 1.84 °C/W and a total thermal resistance of 45.84 °C/W. This resulted in a worst-case junction temperature of 187 °C at an ambient temperature of 25 °C given by (2) and (3).

$$P_{diss} = P_{in} + P_{DC} - P_{out} \quad (2)$$

$$T_j = P_{diss} \times (R_{th} + R_{via}) + T_{amb} \quad (3)$$

Measured Results

The complete schematic of the power amplifier is shown in the Figure 5. The performance results are shown in the Figs. 9-12. The S11 is shown in Figure 7. The region between 5.7 to 5.91 GHz has S11 in the order of -19 dB from measurements. The S21, or small signal gain shown in Figure 8 doesn't follow the simulation results because of the parasitic effects, operating close to transition frequency and incomplete model for NPTB0004. The Nitronex device has an accurate small signal model which works well in terms of matching, but the large signal model at 5.8 GHz fails to meet the performance specifications mentioned in Nitronex datasheet. At lower frequencies in the range of 0-1.7 GHz where parasitic effects don't play an overwhelming role the large signal measurements correlate with the device simulations from ADS. The S22 curve is presented in Figure 9. The output match measurement out performs the simulated results. But this behavior is due to mismatch in S21 performance. The final design performance parameters and specifications are summarized in Table III.

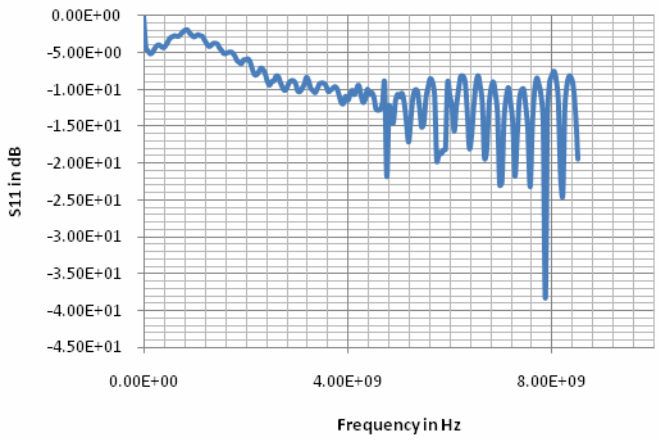

Figure 7 – S11 Measurement result

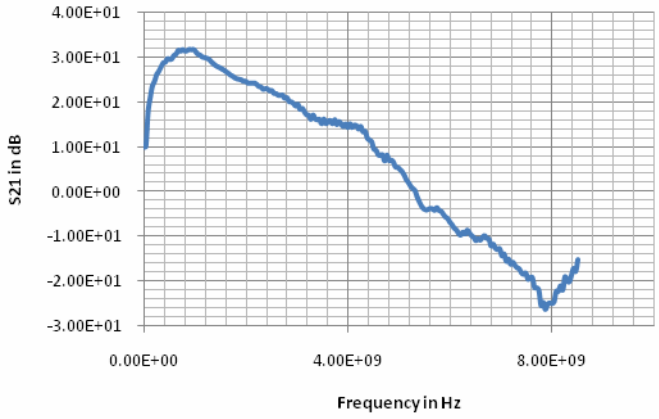

Figure 8 – S21 Measurement result

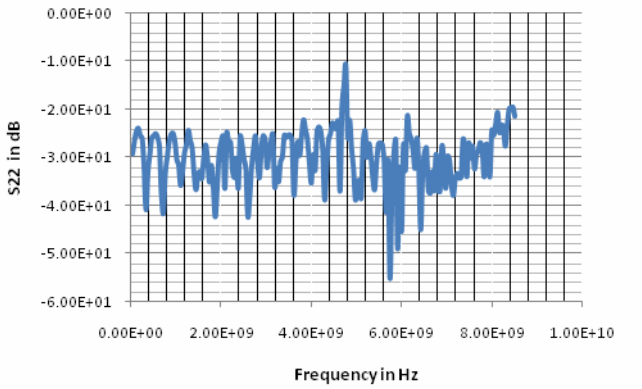

Figure 8 – S22 Measurement result

Conclusions

The power amplifier presented here doesn't meet many of the required specifications. Still a Stable Power amplifier with certain loss of power has been designed with proper matching networks. But working on this design provided a lot on insight into design of power amplifiers and the problems faced when the specifications require designs to be extremely competitive in terms of performance.

The choice of transistor in this power amplifier has influenced the design specifications in an unexpected manner. To make a power amplifier utilizing this device, a wide variety of matching networks should be explored along with an appropriate device modeling in ADS.

TABLE III

PARAMETERS VS. SPECIFICATIONS

Parameter	Symbol	Spec.	Measured Results		
			5.7GHz	5.8GHz	5.9GHz
Input/Output Impedance	Z_0	50Ω	Test Condition		
Drain DC Supply	V_{DD}	24V	Test Condition		
Gate DC Supply	V_{GG}	-1.14 V	Test Condition, I_{DSQ}= 46 mA		
Frequency Range	f_0	5.7-5.9GHz	Test Condition		
Gate DC Supply Current	I_G	≤ 10 mA	6 mA	6 mA	6 mA
Input Return Loss	$\|S_{11}\|$	≤-10 dB	-19.12	-18.76	-18.75
Small Signal Gain	G	> 24 dB	-12.16	-13.36	-14.12
Stability	K	>1	Min = 1.35 from .5 to 7GHz		
Junction Temp at P_{1dB}, T_{amb}=125°C	T_j	≤187 °C	173 °C, worst case		

REFERENCES

[1] "Nitronex Application notes – NPTB0004". Published 2005.
[2] "Design of RF Power Amplifiers " by Steve Cripps.