ECE 6361 - MICROWAVE DESIGN LAB

Project 2: 5.8 GHz High-Power RF Amplifier

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Summary— this report discusses the design of a Power Amplifier circuit using a GaN HFET from Nitronex Corporation – NPTB00004. The design is carried out using ADS software and then measurements are taken using VNA. The device needs to meet a certain number of specifications in the frequency range of 5725MHz to 5850MHz. It needs to be unconditionally stable over a wide bandwidth of 0.1 GHz to 6 GHz. The device described in this report has been characterized in ADS to meet almost all the specifications, except for the gain which was limited due to the inherent limitation of the device model at 5.8 GHz. Scope for further improvement and some issues encountered in the design procedures are detailed in the conclusion section.

I. INTRODUCTION

A Field effect transistor (FET) device needs to be modeled and characterized for use in a one stage RF power amplifier circuitry. The device used is from Nitronex Corporation – NPTB00004 GaN HFET. Its operating frequency range is DC – 6GHz and it is rated for 5 watt. This is a depletion mode FET and it requires negative gate voltage for biasing. The tables below give the test conditions for characterizing the amplifier and the specifications which need to be met.

TABLE I
TEST CONDITIONS

Parameter	*Specifications*
Input/Output Impedance, Z0	*50 ohms*
Drain DC Supply Voltage, V_{DD}	*24 V*
Gate DC Supply Voltage V_{GG}	*0 to -5 V*

TABLE II
DESIGN SPECIFICATIONS

Parameter	*Specifications*
Frequency Range	*5725 – 5850 MHz*
Small Signal Gain	*24dB (Minimum at -10dBm Input)*
Power Output at 1dB Gain Compression	*30 dBm (Minimum)*
Power added Efficiency at Psat dB	*50% (Minimum)*
Gate DC Supply Current	*2 mA (Maximum)*
Input Return loss	*-10 dB (Maximum)*
Stability	*K >1 (DC – 6GHz)*

This report has been organized as follows: section II discusses the design of Power Amplifier using ADS software, followed by section III which discusses measurement procedure, section IV which discusses results, and finally section V ends with conclusions.

II. DESIGN PROCEDURE USING ADS

1) DC Bias

The very first step to design a power amplifier is to find appropriate bias point of the transistor so that it can provide enough gain and effciency. According to the datasheet, the typical bias current for NPTB00004 is 50 mA which requires -1.4 V Vds based on ADS DC sweep simulation (Figure 1).

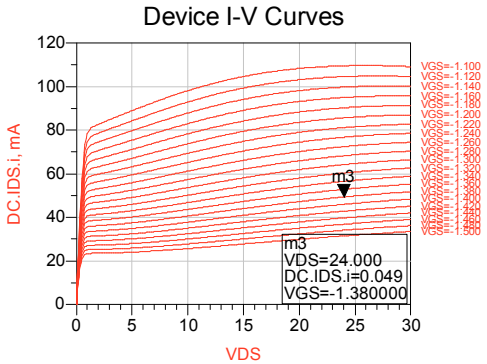

Figure 1: Simulated I-V curves of NPTB00004

2) Optimal Load and Source Impedance

The Power Amplifier circuitry consists of input and output matching networks to match the device impedances to the standard value of 50 ohms. Both the input and output matching networks consist of a series transmission line and a shunt capacitor to match the Z_{IN} and Z_L of the device to 50 ohms. [1] does not provide optimal source and load impedances at 5.8GHz and therefore, the optimal load and source impedances were found out by ADS load and source pull simulation.

The values obtained were
Z_S=70.379-j*141.605
Z_L=12.959-j*15.041

3) Input Matching Network

For matching the input impedance of 50 Ohm to the required source impedance of the transistor, a simple matching circuit with a shunt capacitor was chosen and is shown in Figure 2, to enable flexibility of changing values during hardware matching

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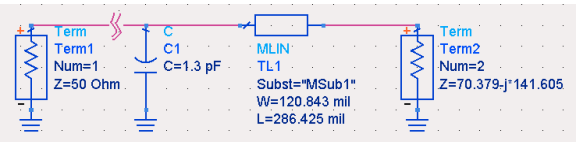


Figure 2: Input Matching Network (Simplified)

The series transmission line length - 286 mil
Shunt capacitor – 1.3 pF

4) Output Matching Network

A similar design was chosen for the input and output matching networks.

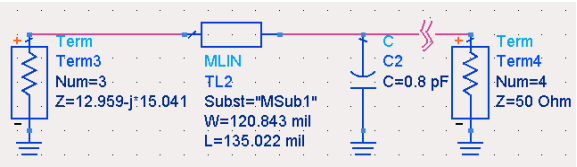


Figure 3: Output Matching Network (Simplified)

The series transmission line length - 135 mil
Shunt capacitor – 0.8 pF

5) ADS Simulation

Bias conditions used
DC supply voltage = 24 V
Gate Bias voltage = -1.38 V (approx)

The corresponding I_{DSQ} – 50 mA (approx - +/- 10 mA variation during measurements)

The bias circuitry consists of passive components. The parasitics associated with some of these components like the Equivalent Series Resistance (ESR), Equivalent Capacitance and Inductance are included in the simulation.

The matching network and the biasing network is added to an existing ADS template and simulated. All the parasitics in the board are included in the simulation, including the shunt stubs on the bias networks (below the Inductor). This schematic is shown in Appendix I. This gives the simulated results of S-Parameter plots, and K- Factor. The S11 plot obtained from simulation is shown in Figure 4. The input reflection loss is seen to be better than -10 dB. The S21 simulated is shown in Figure 6, where there is appreciable gain at lower frequencies and at the required frequency of 5.8GHz, there is negative gain, due to the inherent limitation of the device.

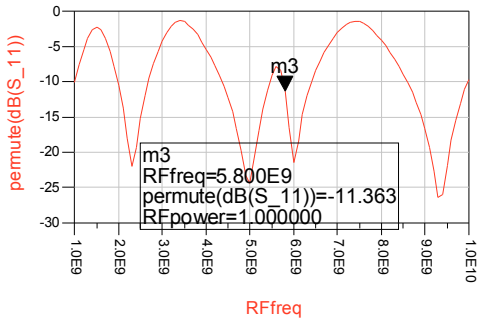


Figure 4: Simulated S11 (for the board layout)

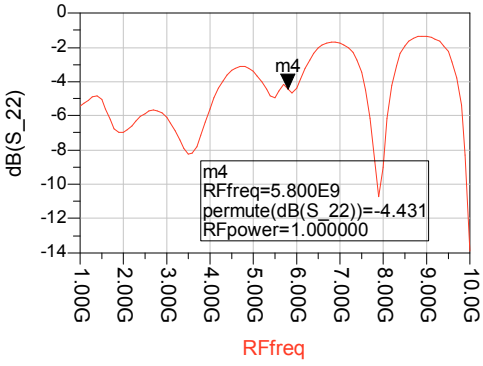


Figure 5: Simulated S22 (for the board layout)

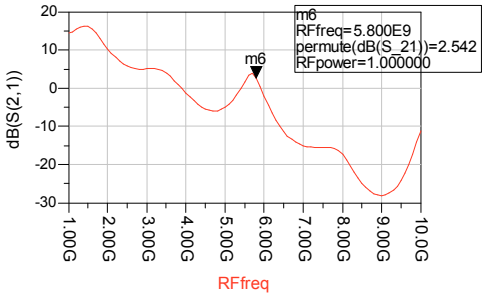


Figure 6: Simulated S21 (for the board layout)

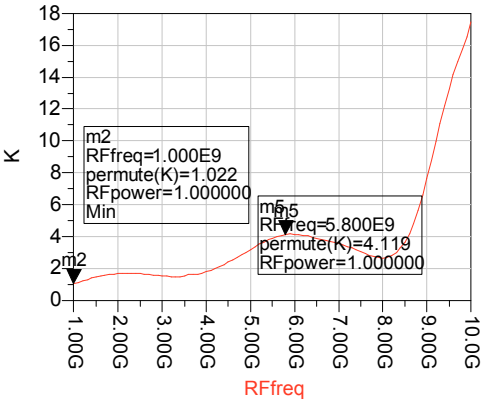


Figure 7: Simulated K factor

The device needs to be unconditionally stable in the frequency range of DC to 6 GHz. This requires K >1 and Gamma < 1. The stability factor K is shown in Figure 7. The minimum value of K is 1.022 at 1GHz.

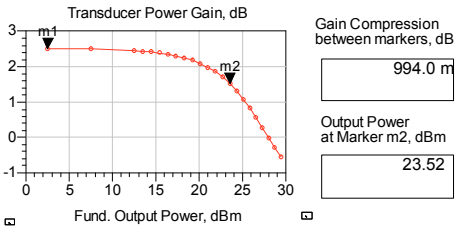


Figure 8: 1dB Gain Compression

The 1dB Gain compression was simulated in ADS by substituting the device model into an existing template. It is seen that the output power level at 1dB compression is 23.52dBm, which is below the needed specifications. Figure 9 shows the power added efficiency vs the input power. It is seen that around 35dBm, the curve becomes horizontal, implying saturation.

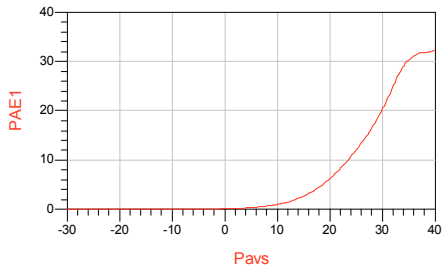


Figure 9: PAE vs Input Power

III. Fabrication and Measurement

Prototype boards were available and the components were soldered on the board. The following table shows the bill of material.

Table 1: Bill of Material

S. No	Component	Value	Vendor	Cost
1	C1	10µF	SMTZone	*Kit
2	C2	1µF	SMTZone	*Kit
3	C3	0.1µF	SMTZone	*Kit
4	C4	82pF	SMTZone	*Kit
5	C5	1.3pF	ATC	0.4$/item
6	C6	0.8pF	ATC	0.4$/item
7	DC Block	100pF	ATC	0.4$/item
8	R1	20 Ohm	SMTZone	*Kit
9	Q1	NPTB00004	Nitronex	23$

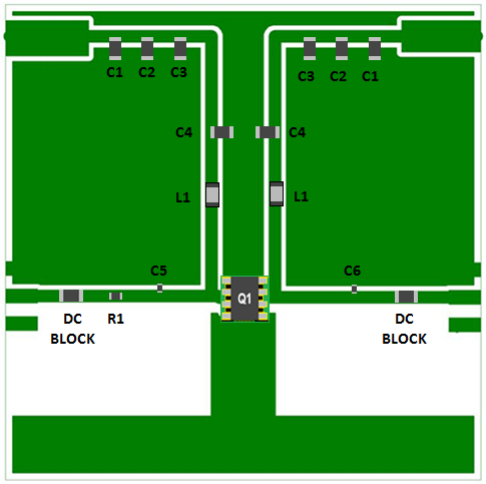


Figure 10: Fabricated Board with Components

The components were populated as shown in Figure 10 on the board.

The S parameters were obtained from a VNA. An attenuator was used for measurement, at the output of the amplifier. The Curves below show the S-Parameters obtained from the measurement. Figure 11 shows S21 obtained without input and output match. It is seen that the S21 obtained at 5.8GHz (-20dB) is far below the specifications. When the input and output match was improved (as shown in figures 12 and 13 respectively) by changing the position of the matching shunt capacitors, after a few trials, there was some improvement in the S21 response. Figure 14 shows the S21 response obtained finally, where at 5.8GHz, the S21 is approximately -0.5dB, which is still far below the specifications.

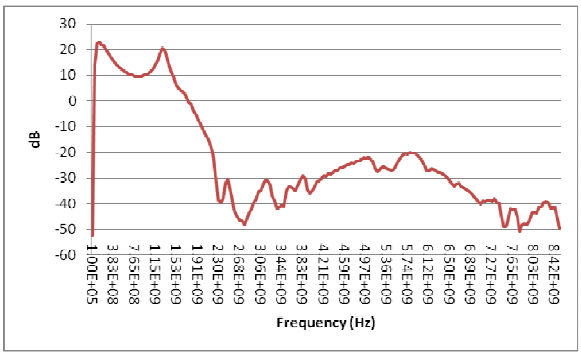


Figure 11: S21 (No Matching)

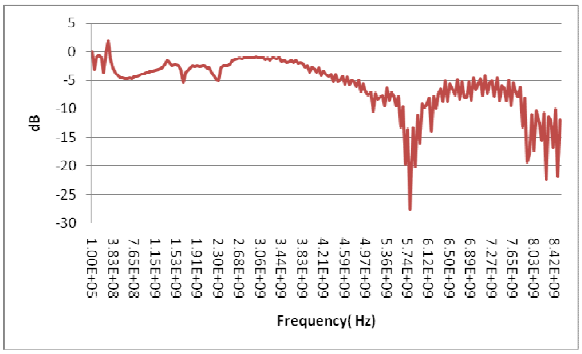


Figure 12: S11

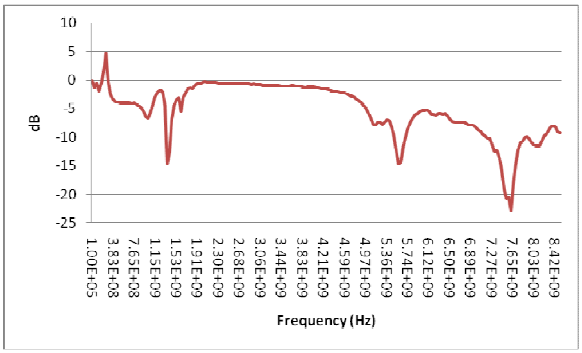


Figure 13:S22

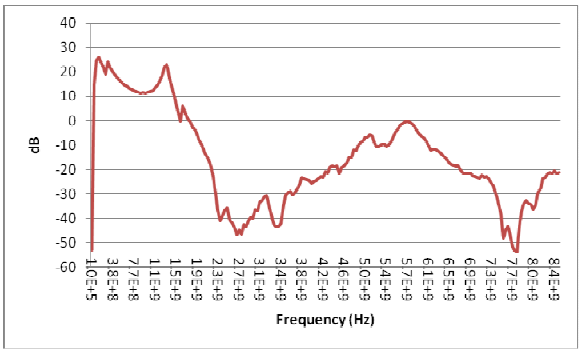


Figure 14: S21 (Matched)

IV. CONCLUSIONS

The specifications have been not met with the design discussed so far. When the device was measured using the VNA, the maximum gain measured was -0.5dB. This is because of the inability of the transistor to perform well at 5.8GHz. From simulations it is seen that stability is still meeting the requirement, K>1. There are spikes and valleys in the measured data. This could be possibly because of variations in the drain to gate coupling in these kinds of devices. Due to the very large transconductance of high-power devices, it is important to minimize any drain-to-gate coupling due to the wires used to connect the devices to the power supplies and to the ammeters and voltmeters. The drain and gate wires should be as far as possible from each other to minimize coupling.

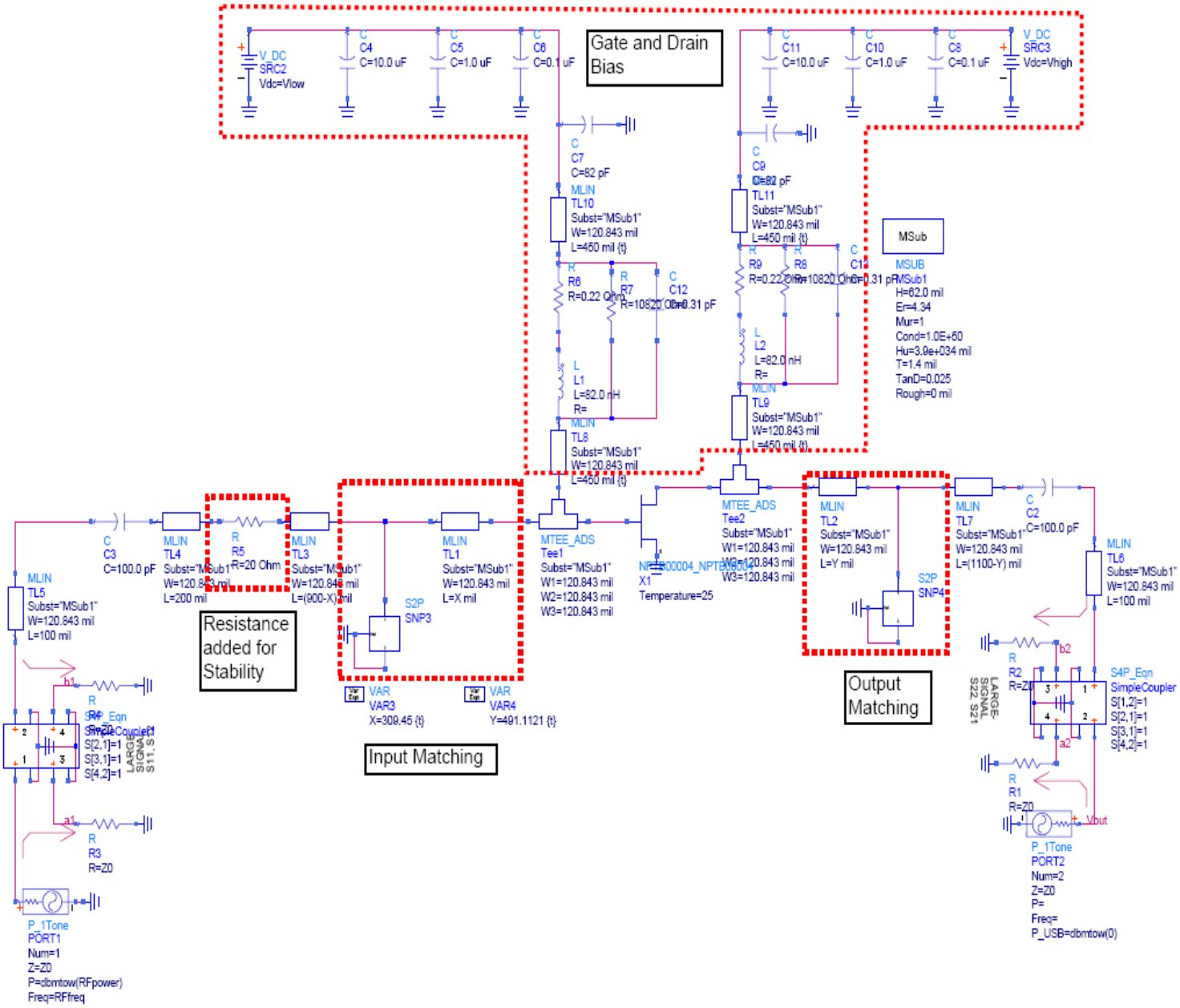
It was also noted that the output of the device was highly dependent on accurate positioning of the matching network, at high frequency. Also the positioning of the RF Block inductor was important in determining the output, since the transmission line below it acts as a Shunt stub. The power amplifier however, is seen to perform well at lower frequencies (below 3 GHz) and therefore it is concluded that the current specifications can be met at lower frequencies or with another device at 5.8 GHz.

REFERENCES

[1] NPTB00004 Gallium Nitride 28V, 5W RF Power Transistor Datasheet, Nitronex Corporation

[2] Agilent EEs of EDA, Presentation on Power Amplifier Design using ADS.

Appendix I



ADS Simulation