5.8 GHz High-Power Amplifier

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I. Introduction

Power amplifier design at microwave frequencies can be quite difficult. First, many devices do not operate correctly at these frequencies. Selecting a package that does not provide parasitic effects requires much research. Second, passive bias components that operate well at microwave frequencies are also difficult to find. Self-resonances must be above the highest operating frequency, or bias and matching networks will cease to function. Finally, much care should be taken to filter out-of-band signals at the input and output, as input harmonics can send the amplifier into an unstable operating regime, and output harmonics can be large and damage following equipment.

In this project, a power amplifier is designed and tested at 5.8 GHz. Design specifications include 24 dB gain, a power-added efficiency (PAE) of 50%, and an output power of 30 dBm.

II. Amplifier Design and Simulation

A. Approach

In this project the target was to design a 5.8 GHz power amplifier with gain of 24 dB and output power of 30 dBm using a gallium nitride transistor (NPTB00004) from Nitronex. First, from the transistor and test board models of transistor and test board available at [1], the transistor's characteristic was simulated in ADS to see how much gain the device can provide. Then load and source pull simulations were performed to have the optimum load Z_L. Afterwards, the P_{1dB}, IMD3, output power, and PAE were acquired.

B. Maximum Gain

First, the simulation was done without any microstrip line or matching components. Only the bias circuit was applied to sweep the Gmax (maximum gain) over the frequency (Figure 1). The gate voltage was -1.38 V and the drain voltage 24 V. Gmax is the highest gain the device can provide. The result in Figure 2 shows a maximum gain of 12.9 dB is available at 5.8GHz.

C. Stability

Next, a stability simulation was performed to ensure the K-factor was larger than 1. The circuit is quite unstable, as can be seen in Figure 3, especially in lower frequencies. Therefore a stabilization circuit is required to prevent oscillation. Series resistors were placed before the gate and after the drain to

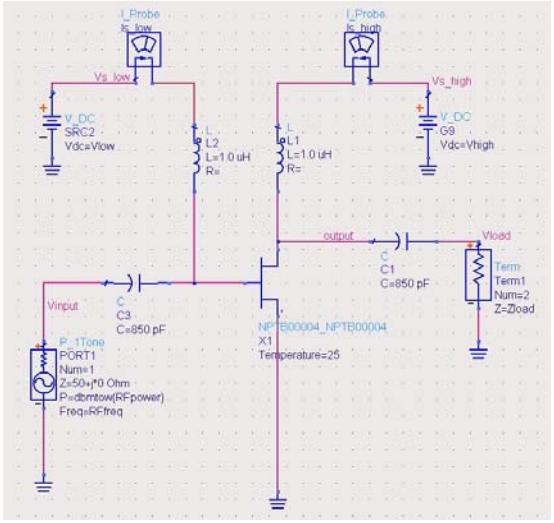

Fig. 1. ADS schematic for simulation of maximum gain.

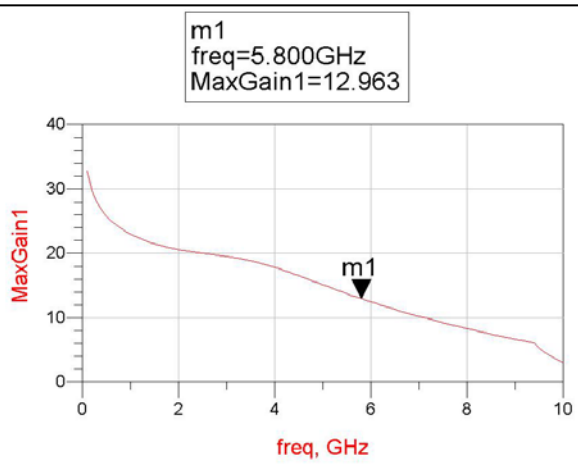

Fig. 2. Gmax of NPTB00004.

increase attenuation through the path signal. Since the circuit is most unstable in low frequency, a resistor was also added from the gate bias to the inductor. The inductor was decreased to a small value to create a low frequency path to prevent oscillation in the corresponding range (Figure 4).

As a result of stabilization, a K-factor larger than 1 over all frequencies is observed in Figure 5. Then the available Gmax was again surveyed. The result shows a gain of only 5.5 dB at high frequency.

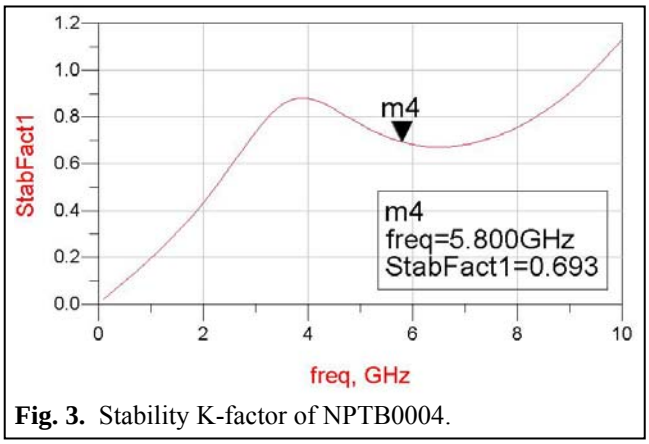

Fig. 3. Stability K-factor of NPTB0004.

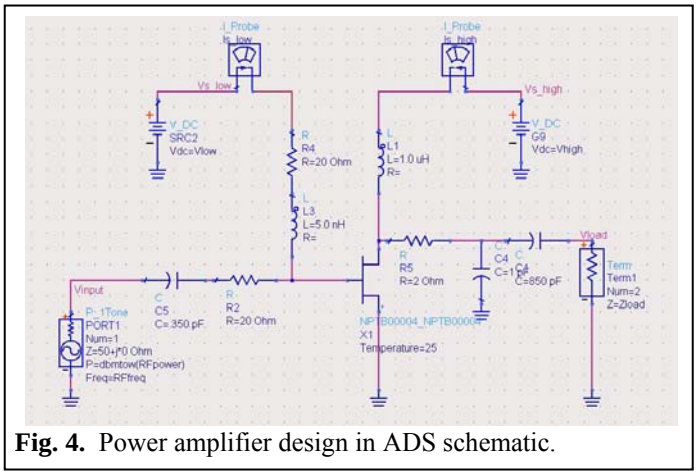

Fig. 4. Power amplifier design in ADS schematic.

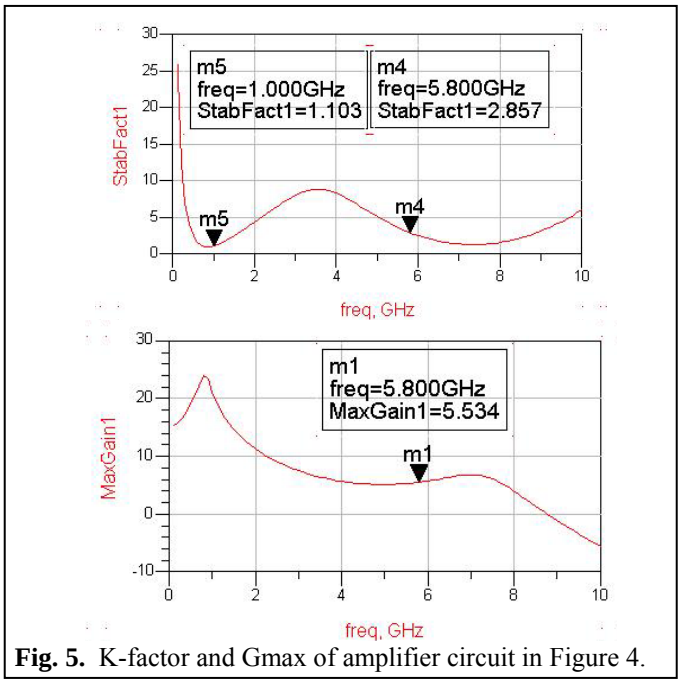

Fig. 5. K-factor and Gmax of amplifier circuit in Figure 4.

D. *Matching*

Attention was then turned to matching. Load pull and source pull simulations were not done because the gain was too low to have a high PAE or output power. Considering the actual loss in FR-4 board and model discrepancy, the gain was expected to be even lower. To determine the matching network, an s-parameter simulation was run to see the input and output impedance on the Smith chart (Figure 6). It shows the input and output are both inductive loads. To simplify the matching we add one series capacitor (0.35pF) at the input and one shunt capacitor (1pF) at the output to complete matching (shown in figure 4). The S11 and S22 are both good at around -10 dB, which is shown in figure 7.

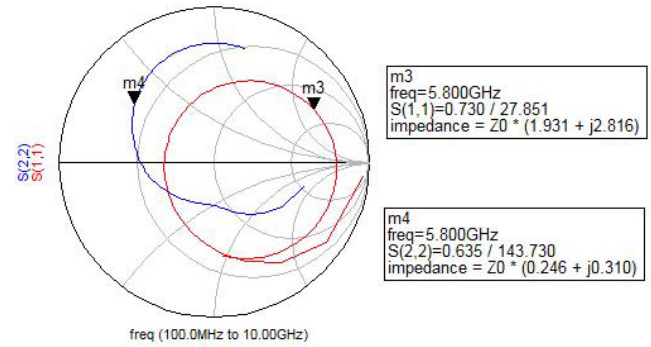

Fig. 6. S11 and S22 of the PA without matching.

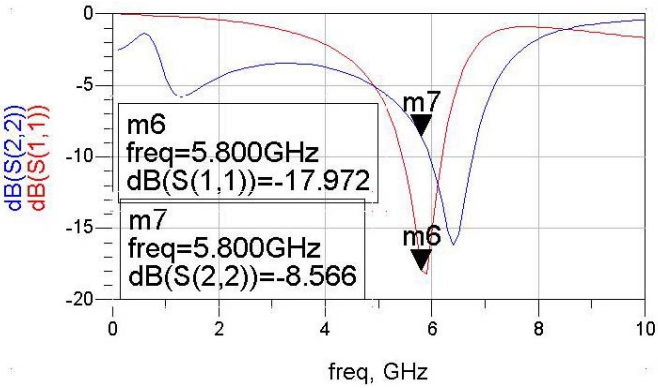

Fig. 7. S11 and S22 of the PA after matching.

E. *Power Sweep and Linearity*

Harmonic balance simulation is used to sweep different input powers to observe the output. The results are summarized in Table 1 and Figure 8.

Table 1. PA Performance with Pin = 26 dBm

Parameter	Value
Output Power	30 dBm
Power Gain	4.9 dB
P1dB (input)	32 dBm
PAE	18%
Psat (Pout @ 3dB gain)	36.6 dBm
IMD3	49.1 dBc

F. *Alternate Design*

In addition to the previous design, another was created with more gain but lower stability. The source and load have been optimized to have the best gain and matching. Load pull and

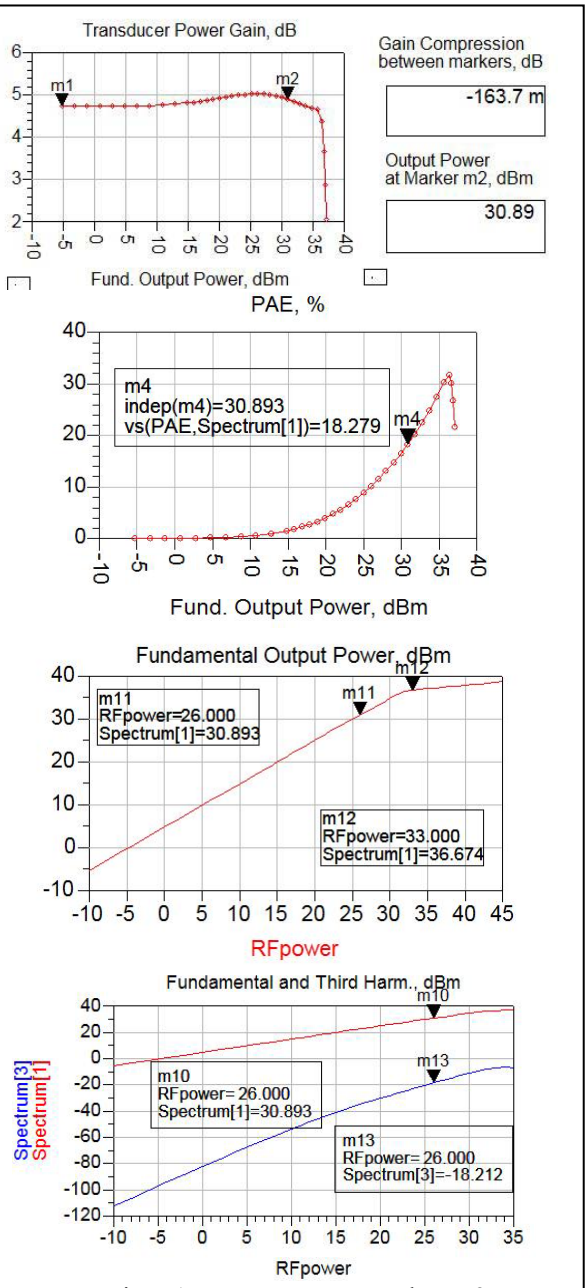

Fig. 8. Power gain, PAE, output power, and IMD3 sweeps.

source pull simulations were used to find the optimum load; by optimization the best loads were selected. Figure 9 shows the schematic of the power amplifier circuits. The power amplifier has been designed for a drain-source current of 50 mA, which is recommended by the datasheet. The output optimum load has been matched to 50 Ω by two capacitors by L-matching. In the gate of the transistor a 20 Ω resistor has been used to make the power amplifier more stable. In the input another L-matching circuit has been designed to match the 50 Ω to the optimum load. Figure 10 shows the S11 of the circuit which indicates that the matching has been done very well in the input and in the desired band the S11 is under -10dB.

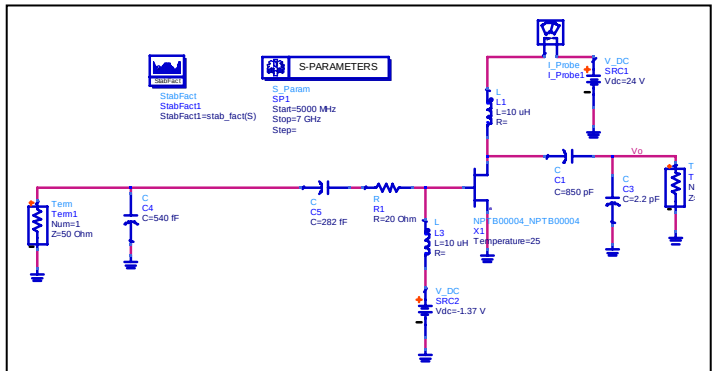

Fig. 9. ADS schematic of alternate PA design.

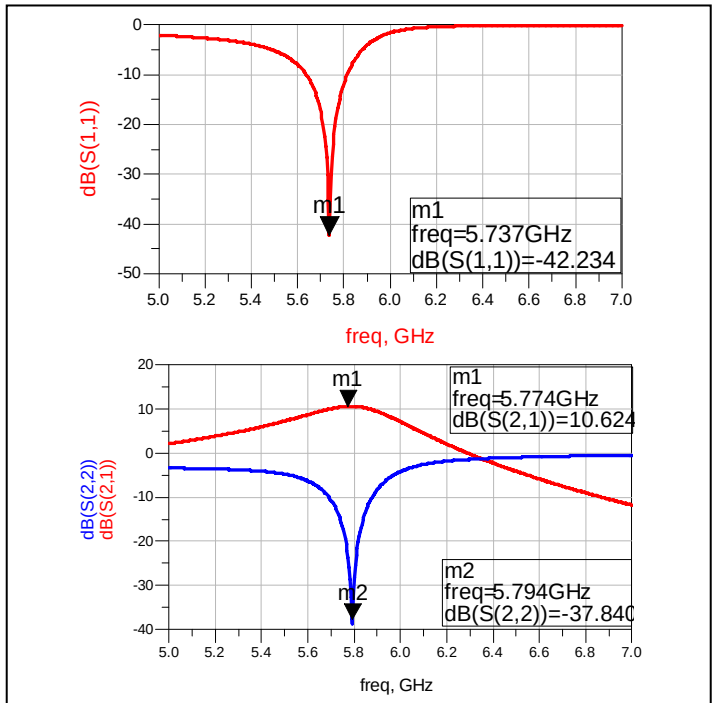

Fig. 10. S11 (top), S21 (bottom red), and S22 (bottom blue) parameters of alternate PA design.

Figure 10 also shows the S22 and S21of the circuit. The S22 shows that the output also has been matched very well. The value of the S22 for the desired band is also under -10 dB. The S21 shows a small signal gain of 10.6 dB in the desired band, which is the maximum gain based on the datasheet of the transistor at this frequency.

It should be noted that this high gain is obtained because the stability factor is low. The stability factor is shown in Figure 11. The stability factor is 1.1, which should be larger than 1 and implies that the amplifier is close to instability.

The time domain signals of the input voltage and output voltage are shown in Figure 11 as well. Based on this figure the input voltage is 2.6 V (corresponding to 18.3 dBm) and the output voltage is 7.88 V (corresponding to 28 dBm). In this case the gain is 9.7 dB and this is the 1 dB compression point. Therefore the gain of the power amplifier is 10.6 dB and the 1 dB compression point is 28 dBm. The DC current of the power amplifier is 111 mA, meaning 2.66 W is consumed at the 1 dB compression point. The brief performance of the power amplifier is shown in Table 2.

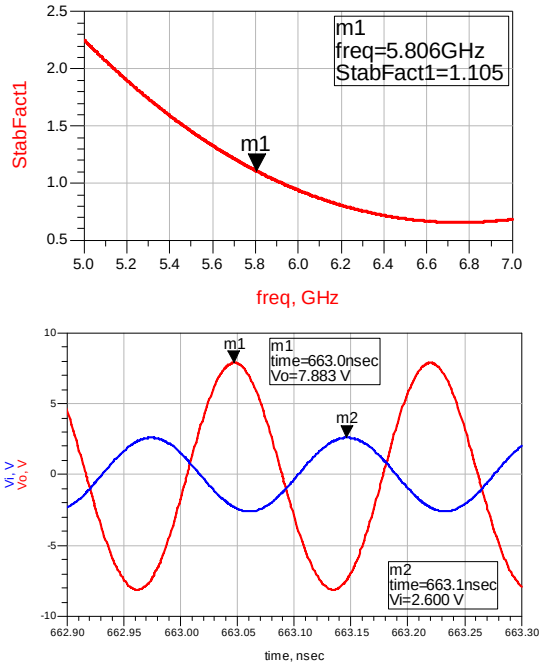

Fig. 11. K-factor of alternate PA design and input/output transient CW signals.

Table 2. Performance Specs for Alternate PA

Parameter	Value
Small Signal Gain	10.6 dB
Power Output at 1 dB Gain Compression	28 dBm
Efficiency	23 %
Power Added Efficiency	21 %

G. Simulation Results

From the simulation conducted in ADS, the best specifications possible for this amplifier at 5.8 GHz are 5 dB gain and 18% PAE to push a 30 dBm output. The gain is so low because of stability issues. It tends to oscillate at frequencies above 4 GHz. The trade-off is to decrease some gain to achieve a stable circuit. Even if the resistor is removed, the highest gain is still only 12.9dB as shown before, which means this device cannot be used to have a 24 dB gain at 5.8 GHz.

III. Measurement

The component values from simulation were used to demonstrate the PA, seen assembled in Figure 12. The result had a very large discrepancy with the design. At 5.8 GHz, the gain was in fact -20dB. The PA apparently had gain at lower frequencies as shown in Figure 13, but it decayed very seriously after 4 GHz. S11 and S22 measurement are also shown in Figure 14. A drop around 5.8 GHz for S11 and S22 is visible, which means the matching network works for the device. The gain cannot be lifted probably due to the device's operating frequency being lower than the specification. Also, the board layout results in lines that are something between microstrip line and coplanar lines; modeling of this line seems

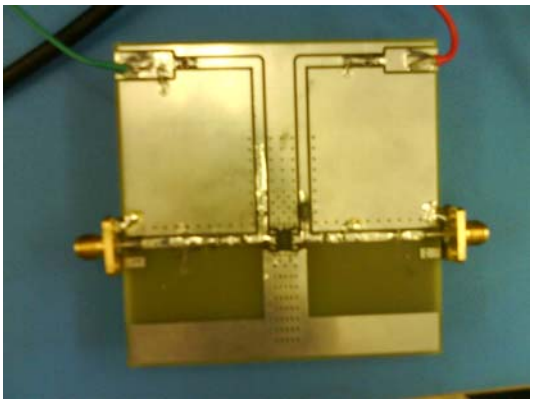

Fig. 12. Assembled PA board.

Fig. 13. S21 for assembled PA.

to be difficult. Regarding the matching, because of limited component values in laboratory, one 0.5 pF capacitor was used in series with a 1 pF to approximate the 0.35 pF in simulation. The result was poor, so this was changed to two 0.5pF capacitors in series.

The other design of PA in simulation was also tried to see if better performance could be obtained. Unfortunately, the measured results were not as expected. It was in fact worse than original one and has a larger discrepancy compared with simulation.

IV. Conclusions

Two different designs were attempted for the PA, but both were not as expected. The reason may be simply because the frequency is too high for the transistor. The measured S-parameter files of the power amplifier from the network analyzer were extracted to compare the result with previous simulations. Figure 15 shows the Gmax sweep of power amplifiers using models from simulation and measurement. At lower frequency, these two lines are quite similar, while in higher frequency they deviate greatly. Although the data sheet says its frequency range is 0-6 GHz, it should be more suitable for operation in an amplifier mode at less than 4 GHz because it is clear there is gain only under 4 GHz through

measurement.

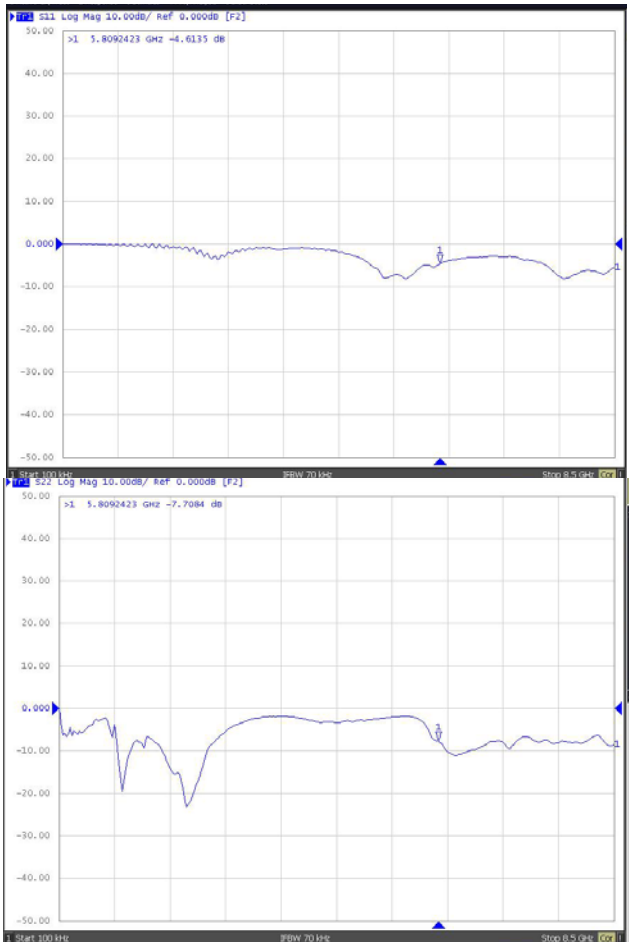

Fig. 14. S11 (top) and S22 (bottom) for assembled PA.

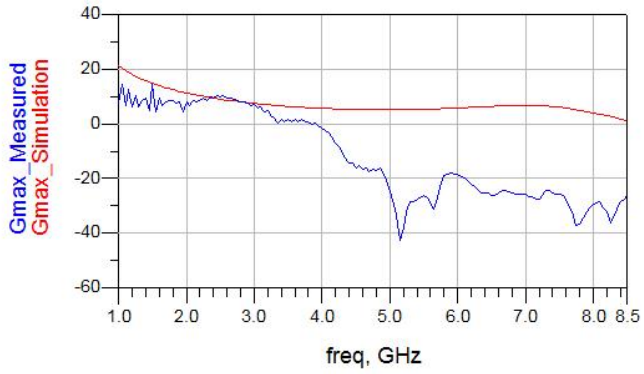

Fig. 15. Gmax comparison of simulation model to actual measure s-parameter data.

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