5.8 GHz High-Power RF Amplifier

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July 2010

I. INTRODUCTION

POWER amplifiers (PAs) are high-frequency amplifiers that are designed to output especially high amounts of power, typically on the order of 1 Watt or higher. A PA is generally used as the stage preceding the antenna in a wireless transmitter. PAs boost the strength of the signal to be transmitted so the antenna can broadcast the signal over a larger range. Two prime considerations in PA design are output power and linearity. A high output power predictably increases the transmit power of a circuit. A highly linear PA can output strong signals without distorting them in either the time or frequency domain. PAs do not necessarily require high gain. The primary goal of a PA is to output high power signals, not to amplify weak signals. According to Steve Cripps, "PAs are amplifiers whose outputs either directly or indirectly make an impact on the human sensory system" [1]. Because PAs deal with such large RF signals, they consume a large amount of DC power, which generates a significant amount of heat. An important consideration in PA design is thermal management. Reducing the amount of DC power consumed by the PA means less heat is generated. Therefore, maximizing the efficiency of a PA is a key design objective. PAs are large-signal circuits, which makes them difficult to model accurately and design.

II. DESIGN

The goal of this project is to create an SMA connectorized board that will interface with a Mimix XP1039-QJ GaAs FET two-stage PA [2]. The board must be able to dissipate the large amount of heat that is generated by the PA.

A. Biasing

The transistors used in this PA are p-type GaAs FETs. Thus, the gate terminal must be biased to a negative voltage before a drain voltage is applied. If a drain voltage is applied without a negative gate voltage, the device will be destroyed. The recommended bias voltages for this PA are around -0.7 V for each gate and 8 V for each drain. When fully biased, the first stage should draw 466 mA and the second stage should draw 933 mA. This PA therefore dissipates 11.2 W of DC power. Clearly, this amount of power in such a small package will lead to thermal issues.

In order to properly and safely bias this PA, a Maxim MAX881R Low Noise Bias Supply for GaAs FET PAs is implemented [3]. This chip takes a 5 V input and sets the desired negative voltage on the gate using an external resistor divider. Once the gate is 92.5% charged, an active-low power OK signal (~POK) is triggered. The ~POK signal drives the gate of an International Rectifier IRF5305S Power P-MOSFET that acts as a switch [4]. When ~POK drops, the PFET connects the drain pins of the PA to the 8 V drain supply. This chip ensures that the PA is always biased to the correct levels and cannot be destroyed by biasing the drain before the gate. An LTspice schematic of the bias chip interfacing with the PA is shown in the Appendix.

B. PA Implementation

The provided PA is fully integrated and matched to 50 ohms, so matching networks are not necessary. No model files are available online, so the PA cannot be simulated. 50 ohm microstrip lines are used to connect the RF_{in} and RF_{out} pins on the PA to the SMA connectors. LineCalc estimates that these lines should be 56 mils wide.

According to the XP1039-QJ PA datasheet [2], the output power of this PA is 4 W, or 36 dBm. The small-signal gain is 16.5 dB, P_{1dB} is 35.5 dBm, and the output-referred third-order intercept point (OIP3) is 49 dBm. The gain on this PA is not especially high, but, as mentioned earlier, the output power of the PA is more important than the gain. The P_{1dB} and OIP3 are high, so this PA is highly linear. The efficiency of this PA (P_{out}/P_{DC}) is 35.7%, and the power added efficiency (PAE) ($(P_{out} - P_{in})/P_{DC}$) is 24%. The efficiency depends only on output power, so it will generally be large for a PA. PAE, on the other hand, depends on the gain of the PA, so it will be lower than the efficiency for lower-gain amplifiers.

C. Board Layout

The primary concern in the layout of the PCB for this PA is heat dissipation. Because this PA dissipates 11.2 W of DC power, proper heatsinking is required for this PA to operate properly. In order to remove this heat, the primary ground traces for the PA are made wide and connected to the ground plane on the underside of the FR-4 through multiple vias. The board layout is shown in Fig. 1. 50 ohm lines are used to connect the PA to SMA connectors. Metal pads are used to

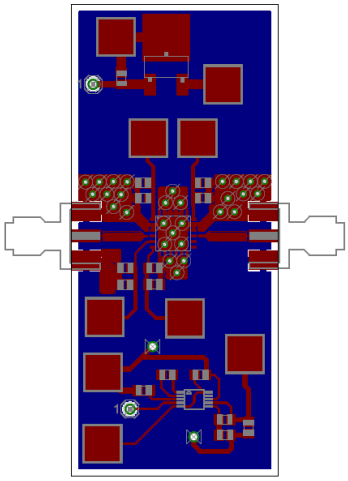

Fig. 1. PA board layout.

connect to all DC bias lines and the ~POK signal from the bias chip. The bias chip and pFET are not directly connected to the PA on the board so the PA biasing can be tested manually. If the PA can be successfully biased, wires can connect the bias circuit to the PA.

The board was milled using a T-Tech Rapid Circuit Prototyping System in the Georgia Tech School of ECE in-house facilities. The substrate was 31 mil FR-4 with 1 oz copper traces. Components were soldered onto the board by hand using solder paste and a reflow oven. Vias were plated by inserting a wire into each hole, filling the gaps with solder paste, and curing the paste using a hot air gun. After the board was fully soldered, additional heat sinking was implemented by soldering four 22-gauge wires to the ground plane near the PA chip. These wires were soldered to copper mesh in an attempt to provide a path for heat to leave the board. A picture of the fully soldered board is shown in Fig. 2.

III. Results

Unfortunately, the PA could not be biased up correctly. -0.7 V was applied to the gate, and the drain voltage was stepped up starting at 4 V. The PA drew around 1 A, and the gate bias shifted slightly as the drain voltage was increased. The voltage suddenly dropped to nearly 0 V while the current was at compliance, and subsequent testing showed that the drain terminals were shorted to ground. The device most likely broke down due to excessive current. The heat of the device was not tested, but the PA may have broken down because of excessive heat.

The PA chip was desoldered and a new chip was soldered to the board. In an attempt to improve the heatsinking, the wires connecting the ground plane to the copper mesh were desoldered from the board. Copper mesh was then directly soldered onto the ground plane in an attempt to draw more heat out of the ground plane. The gate was once again biased to -0.7 V and the drain terminals were immediately biased to 8 V. The drain current complianced at 1.6 A, dropped down to around 1.3 A, and then shot back up to 1.6 A all in the span of a few seconds. The PA was extremely hot to the touch. The PA was tested and the drain terminals were once again shorted to ground. Because the PA could not be biased up, the bias circuit and the RF performance of the PA could not be tested.

The most likely cause of failure is insufficient heatsinking. Dissipating 11.2 W of DC power in such a small chip creates a large amount of heat in a very small area. The heatsinking could possibly be improved by implementing wider ground planes that extend away from the device. An actual heatsink could be used on top of the chip, and thermal grease such as Arctic Silver could be applied to ensure a robust thermal connection between the chip and the heatsink. The heat probably would not have been an issue if the drain was biased up from ground very slowly. Immediately biasing the drain at 4 V or higher creates a significant amount of heat very rapidly. The PAs soldered onto this board were free samples, so it is possible that these PAs did not meet the designed specifications and are less robust than purchased PAs.

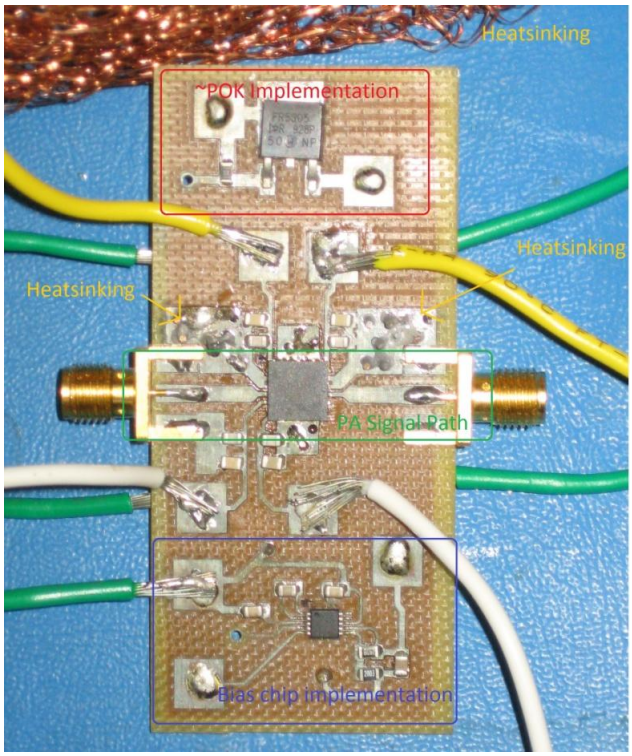

Fig. 2. Populated PA board with heatsinking.

IV. Future Work

In order for future iterations of this project to be more successful, the PCB needs to be designed to conduct heat away from the PA more effectively. The use of an actual heatsink or a cooling system would help dissipate heat and hopefully make it possible to bias the device at the full 8 V drain voltage. The PCBs and vias would be of a higher quality if they were sent out to be fabricated by an external company. The manually plated vias were very low quality, and if the board was fabricated by an outside company, they may conduct heat away from the PA much more effectively. Using a pick and place machine to solder components to the board would result in higher quality electrical connections and would prevent inexperienced solderers from damaging the board. Thermal issues would also be minimized by

implementing a PA that generates less heat. This could be accomplished by using a PA with a higher efficiency, a lower output power, or both.

V. Conclusions

A 5.8 GHz GaAs integrated PA was implemented on a custom PCB with a bias control circuit. The bill of materials (BOM) for this project is in Table 1. The PA could not be biased up, most likely because it overheated. Thermal management is clearly one of the most important yet overlooked aspects of PA design. This PA has been demonstrated to work, so improved biasing techniques and heat dissipation would ensure a functional PA. Despite the failure, the authors learned much about the intricacies of PA design and layout.

Item	Part	Manuf	Cost	Qty	Item Cost
1	PA Chip	Mimix	$0.00	1	$0.00
2	Bias Chip	MAXIM	$5.73	1	$5.73
3	pFET	IRF	$1.13	1	$1.13
4	SMA	Emerson	$5.10	2	$10.20
5	0.22uF	Mouser	$0.11	2	$0.22
6	4.7uF	Mouser	$0.12	1	$0.12
7	100pF	Mouser	$0.02	4	$0.08
8	1uF	Mouser	$0.09	4	$0.36
9	200kΩ	Mouser	$0.04	1	$0.04
10	80kΩ	Mouser	$0.04	1	$0.04
11	100kΩ	Mouser	$0.04	1	$0.04
					$17.96

Table 1. Bill of materials for the PA.

Acknowledgement

The authors would like to thank James Steinberg and Edgar Jones for their assistance in fabricating and soldering the boards for this project.

References

[1] S. C. Cripps, RF Power Amplifiers for Wireless Communications, 2nd ed. Norwood, MA: Artech House, 2006.
[2] Mimix, “5.6-7.1 GHz Linear 4W Power Amplifier,” XP1039-QJ datasheet, Oct. 2009.
[3] Maxim, “Low-Noise Bias Supply in µMAX with Power-OK for GaAsFET PA,” MAX188R datasheet, Jan. 2004.
[4] International Rectifier, “HEXFET Power MOSFET,” IRF5305S datasheet, Apr. 1999.

Appendix

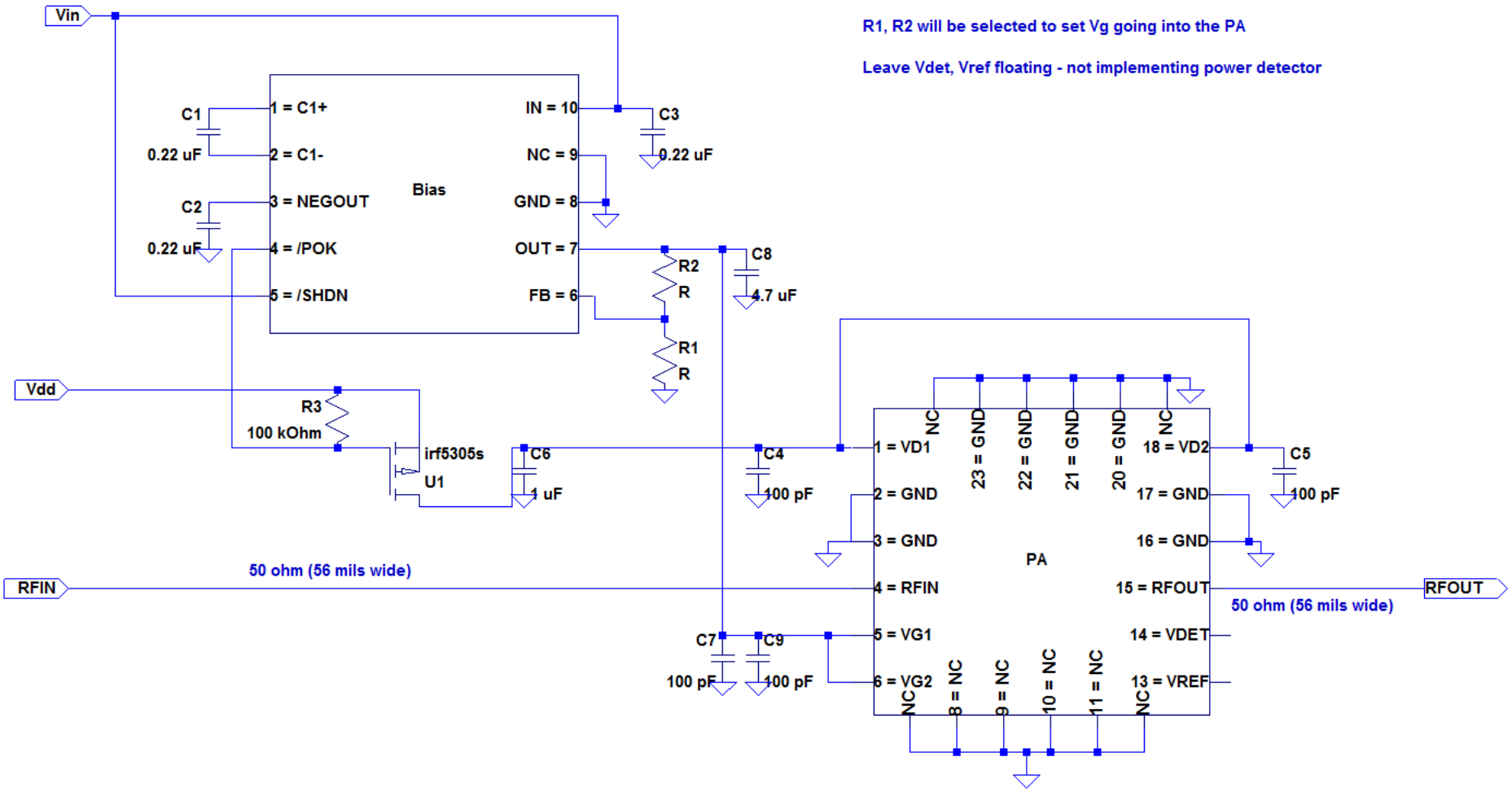

Fig. A.1. LTSpice schematic of PA and bias circuit.