5.8 GHz RF Energy Harvester

Jonathan Parks, Saravanan T K, Yun Zhang & Grant Lohsen

***Abstract* -This paper gives a step-by-step account of the design, assembly and testing of a Schottky charge pump used to convert RF energy at 5.8 GHz to DC voltage. A 4 stage charge pump design is shown here with appropriate matching networks.**

***Index Terms*—RF Energy Harvester, RFID Transponder**

Introduction

The Silicon – Titanium based Schottky diode has been primarily used in RFID transponders. The RFID transponder receives RF energy which is converted to DC Supply voltage using a Voltage multiplier circuit.

Charge Pump

The charge pump circuit presented here is a AC to DC converter. The main requirement of this circuit is to maximize voltage conversion efficiency. The AC to DC converters can be classified as bootstrapped converters and voltage multipliers.

The voltage multiplier is a circuit used to convert AC power to DC voltage using capacitors and diodes. The architecture employed here is a Villard cascade voltage multiplier originally proposed by Heinrich Greinacher shown in Figure 1.

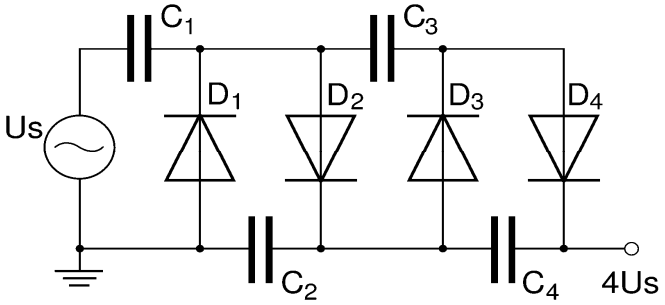


Figure 1. Schematic of Villard Voltage Multiplier

Assuming the peak voltage 5.8 GHz RF signal is Us the circuit charges the capacitor C1 to Us through the diode D1 during the negative half cycle of Us. During the positive half cycle potential of C1 adds with the source which charges the diode D2 to 2Us. The potential at C1 drops to zero leading C3 to be charged to 2Us through D3 during the negative half cycle of Us. The next positive half cycle of Us, the output voltage at C4 reaches 4Us. In reality more than 4 cycles are required to reach 4Us because of the threshold voltage requirements of the diode. The operation of the voltage multiplier is presented in the form of schematic in Figure 2.

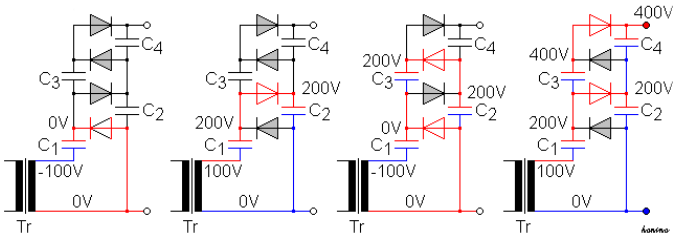


Figure 2. Operation of Voltage Multiplier.

The diodes used in our current circuit are silicon titanium anti-parallel Schottky diodes with low series resistance of 300 Ohms and junction capacitance of less than 15 pF. The input impedance of this diode is dependent on substrate and parasitic capacitances. For typical operating points the real part of the impedance is almost 30 times the imaginary component. The input capacitance has a Q factor of 30 which places high demands on the antenna. A solution to this problem can be obtained by designing a wideband matching network optimized to obtain maximum power efficiency. This requires careful layout of the matching networks to ensure minimal loss at all parts.

LED Modeling

The LED used in this application was modeled first with the help of measurement of I-V characteristics. The voltage versus current characteristics for this diode was measured and stored as a S2P file. The S2P file was then converted into a non-linear equation model in ADS. The necessity for modeling is the non-linear behavior of the diode and threshold voltage requirements to turn on the light emitting diode. Figure 3 shows the impedance versus diode voltage plot for the LED.

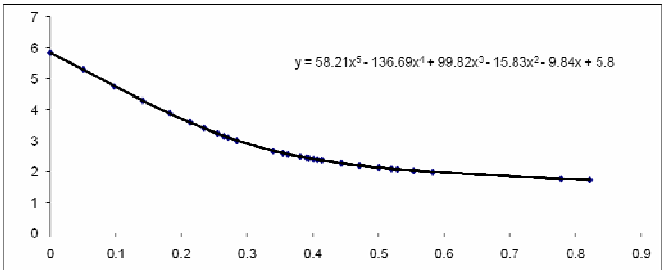
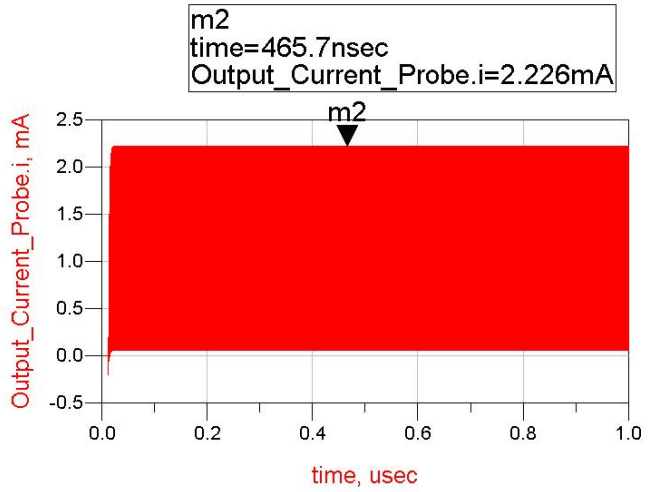


Figure 3. Impedance vs Voltage plot for the LED

Circuit Design

The charge pump circuit was devised into three different designs of varying number of stages. A 3 stage, 4 stage and 5 stage design were designed and simulated in ADS. The 3 stage charge pump circuit was seen to burn more current through the LED. Since the brightness of the LED is dependent on the current flowing through a 3 stage design would be optimal for a LED with low turn on voltage. A 5 stage design is optimal for generating high voltage which is necessary for a device with a high turn on voltage and low current requirements. A fair compromise between the two ideas would be to put in a 4 stage design. The schematic of the 4-stage charge pump circuit is shown in Appendix A, Figure A1. The corresponding current and voltage plots for the charge pump circuit design are shown in Figure 4.



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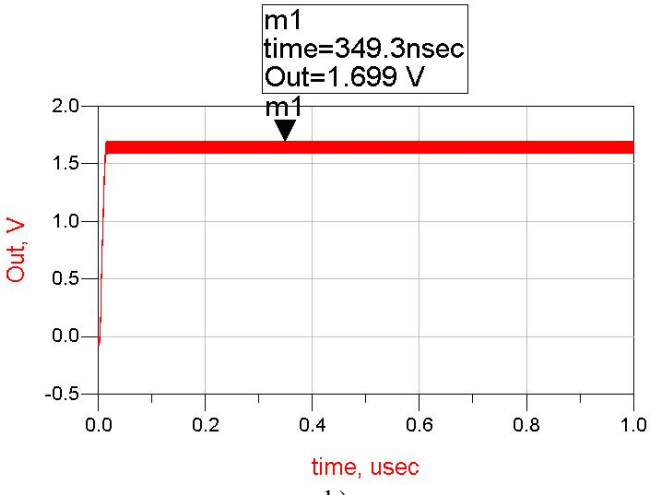


b)

Figure 4. Consumption for 4 stage charge pump circuit design a) Current across LED b) Output Voltage

Matching Network Design

Designing a matching network for the 4-stage charge pump was a very difficult task, due to the non-linearity introduced by the diodes. As a first pass, it seemed intuitive to match the input of each diode in the charge pump circuit to 50Ω, and then to design a power divider at the same impedance for delivering the RF signal. However, after many simulations, it was found that equivalent or better performance was obtained through simple designs without complex matching networks.

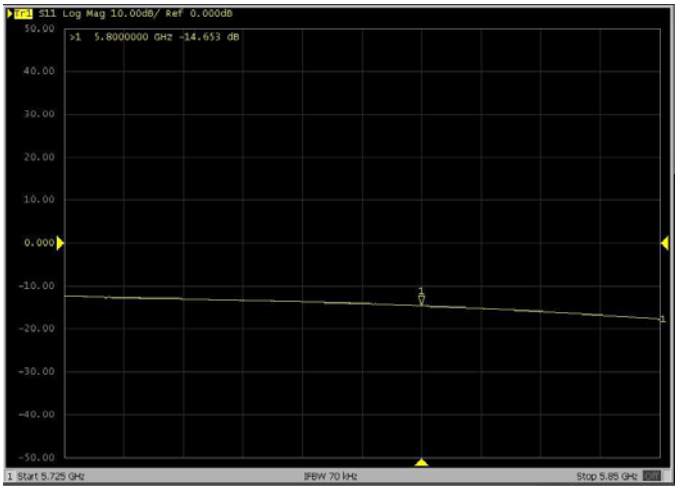
In the end, the individual matching network theory was abandoned in favor of a broadband matching network used to transform the Real load impedance. This was implemented as a quarter-wave transformer. In case additional matching was necessary, a length of 50Ω line was left between the transformer transmission line and the SMA connector. Here, stubs could be added for improved matching.

Layout

After simulating in ADS, the charge pump circuits were designed in Eagle Layout Software, as seen in Appendix A, Figure A2. In the figure, notice that a total of six circuits were included in the layout. Here, two layouts for each stage number (e.g. 3,4,5) were included, with one layout having a transformer stub, and the other having pads for a discrete component matching network. This diversity was a strategic move in offering multiple contingency plans in case the original designs were unsuccessful. Despite this planning, only the four stage layouts were fabricated.

Conclusions

Of the six layouts, the 4-stage charge pump with the quarter-wave transformer was first assembled on the PCB. Using a network analyzer, it was determined that the LED could be lit with 4.5dBm of input power. While performing this test, the S11 parameters were measured, and can be seen in Figure 5.



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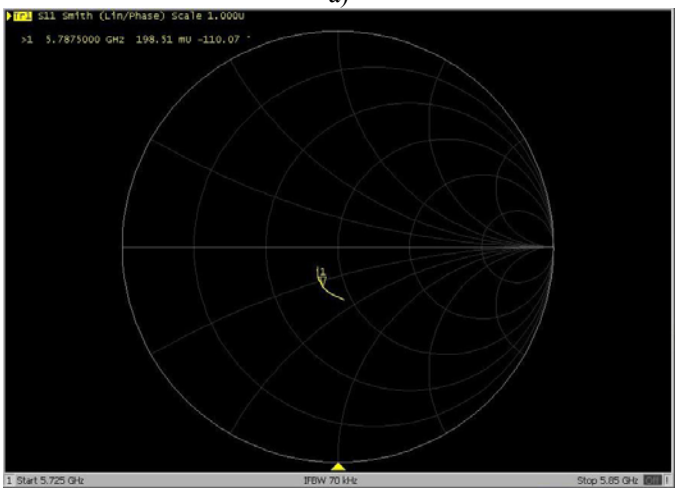

b)

Figure 5. S11 Parameters for 4-stage charge pump

Notice that a return loss of -14.653 dB was measured at 5.8GHz. This was considered a very successful match, and thus no further manipulations were deemed necessary.

Note: The layout seen in Appendix A, Figure 2 was designed for a FR-4 PCB with a thickness of 62 mil, however the design was mistakenly fabricated on 32 mil board. When taking the S11 measurements, a drastic null was noticed in the return loss around 4 GHz, which is assumed to be the primary minima associated with our matching network. However, since stub matching is harmonic in nature, another minima was observed at the design frequency. Since this occurrence was not planned, it can be most certainly be said that "… in engineering, you have to be smart enough to know when you're lucky."

Appendix A –Schematics and Layouts

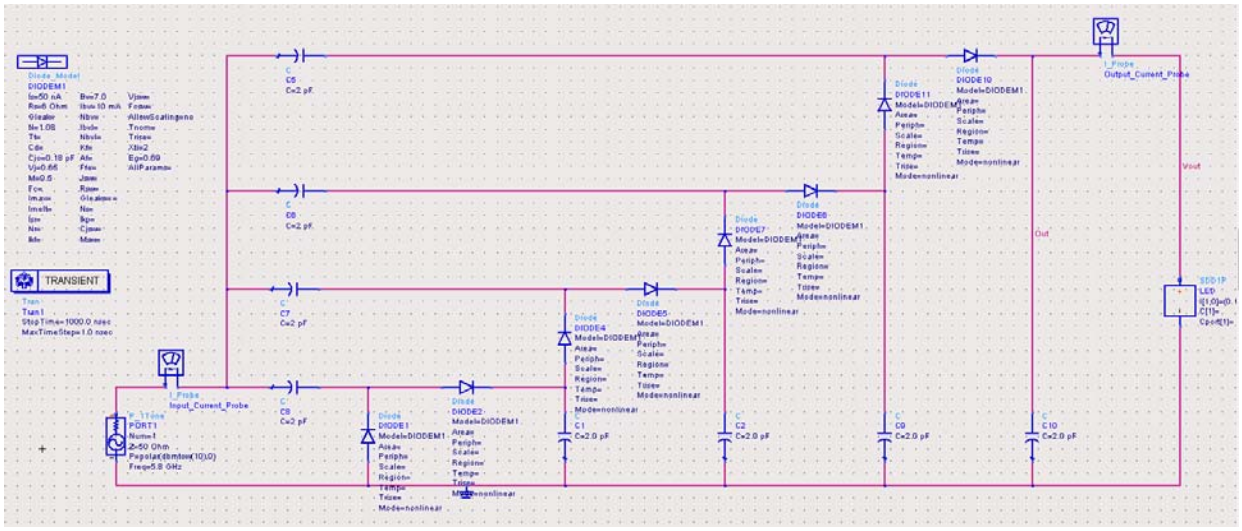

Figure A1. ADS Schematic of the 4 stage charge pump circuit design.

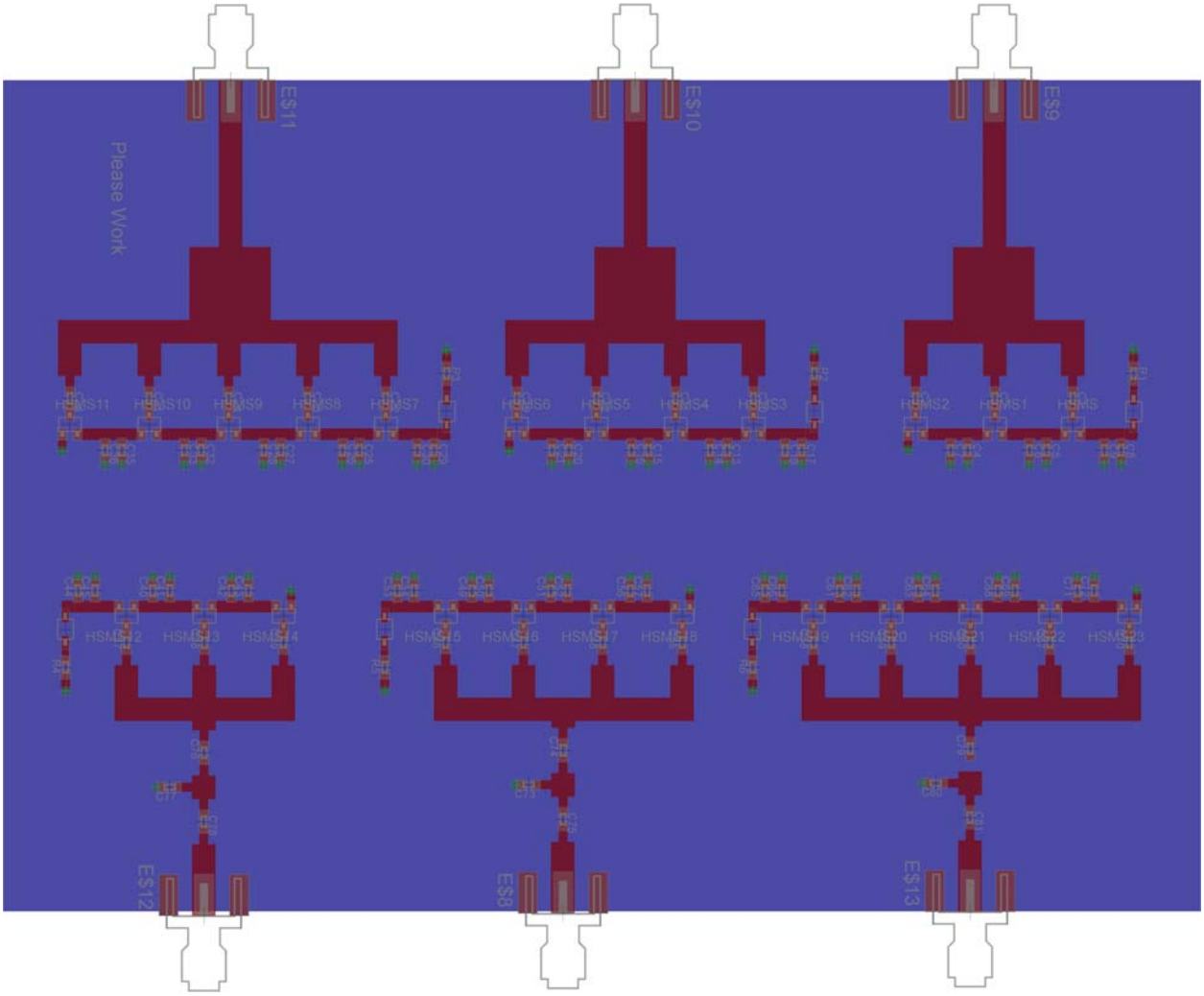

Figure A2. Charge Pump Eagle Layout