Project 3: RF Energy Harvester

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I. Overview

For this, the third project of ECE 6361, a device is to be designed and implemented to power an LED from a 10 dBm, 5.8 GHz input signal. This input is to arrive at the device via a 50 Ω line. The voltage required to turn on the LED will be greater than the input voltage, so a voltage multiplier will be necessary. In this case, a charge pump will be used to increase the voltage, the design of which is discussed in section II. Using a charge pump also necessitates dividing the incoming signal, which is covered in section III. The design chosen for implementation is detailed in section IV.

II. Charge pump design

A. Broad overview

There are many methods available for rectifying AC signals, perhaps the most basic of which is the half-wave rectifier. This uses a diode to remove the negative part of the cycle, and a capacitor to 'buffer' the signal between the positive parts of the cycle. This will produce a peak output voltage of $V_A - V_T$, where V_A is the voltage across the antenna and V_T is the diode turn-on voltage. This design throws away the negative half of the received signal.

An improvement on this is the full-wave rectifier. This operates in the same manner as the half-wave rectifier when the incoming signal is positive, but when the incoming signal is negative, a positive signal is pulled up from ground onto the input capacitor and then pushed onto the load (and output capacitor) on the following positive cycle. This results in a doubling of the output voltage.

This idea can be further extended to increasing the output voltage N-fold, as illustrated in figure 1. The analysis of this type of circuit is very similar to that of the Dickson Charge Pump, described in detail in [1]. Comparison of figure 2 with figure 32 from [1] should make this readily apparent.

A full and detailed analysis of the operation charge pump with a sinusoidal input is beyond the scope of this work, but it can broadly be understood by considering operation where a simple square-wave input is provided. On the very first negative cycle (figure 2a), a potential difference is created across C_1, C_2 and C_3. When the following positive cycle occurs, the potential differences created in the first cycle will combine with those from the second to create a potential difference greater than V_{in} across C_1 and C_2, and to produce a voltage across C_3 and the output. In each successive cycle, the potential difference left across the capacitors from the previous cycle combines with the input voltage to produce higher potential differences across the capacitors higher up in the chain. Charge is "pumped up" to the load. After many cycles, this reaches a steady state, where the voltage at the output is four times that across the first stage, and the voltages at the lower stages are reduced accordingly. This basic idea can readily be extended to N-stage charge pumps.

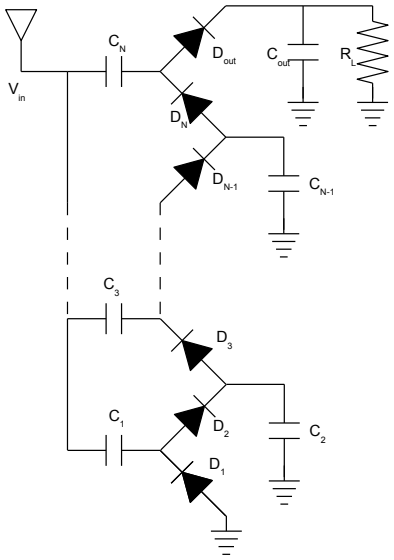

Fig. 1. An n-stage chargepump (for N odd). If N is even, then the Nth diode is connected to the output diode as above but, with the Nth capacitor being grounded and included as a stub between the Nth diode and the output diode.

B. Design Equations

The key purpose of the charge pump (at least in this application) is to produce a rectified output voltage greater than the input voltage. Trotter [1] gives the steady-state output voltage as:

$$V_{out} = \frac{(N+1)(V_{in} - V_t)}{1 + \frac{N}{fCR_L}} \tag{1}$$

where V_t is the turn-on voltage for the diodes used in the circuit and N is the number of capacitor-diode pairs, excluding the output capacitor and diode. Note that at high frequencies and at least moderate loads, $\frac{N}{fCR_L}$ will become small, leading to the approximate expression:

$$V_{out} = (N+1)(V_{in} - V_t) \tag{2}$$

For square-wave input, V_{in} is simply the peak voltage. However, in the case of a sine wave its meaning is rather more complicated - the voltage left across each capacitor as the diodes turn off will be a function of capacitance, frequency and diode impedance. For the purposes of calculation here V_{in} is approximated by the RMS input voltage. This was found to be reasonable in some Spice simulations, but it has not been thoroughly tested, and its validity is open to question.

Trotter [1] also provides a procedure for choosing component values. This procedure is presented in a slightly modified

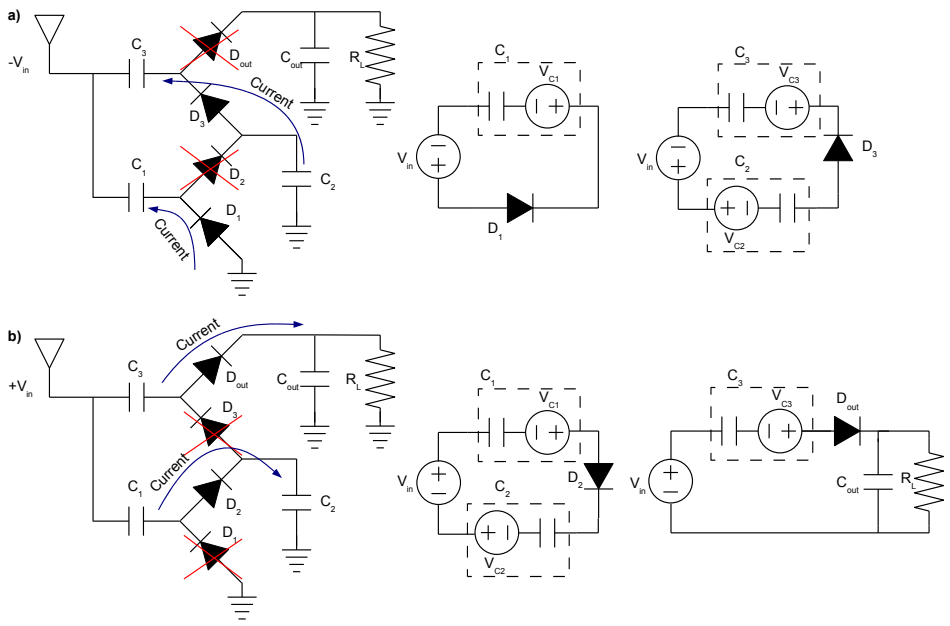

Fig. 2. A three stage charge pump, along with equivalent circuits for the two different basic modes of operation. **a** shows the behavior of the charge pump when V_{in} is negative and **b** shows the behavior when V_{in} is positive.

form here. The load impedance R_L, input voltage V_{in}, diode turn-on voltage V_t, number of stages N and frequency f are all assumed to be predetermined. The value of the $C_1 \ldots C_n$ is given by:

$$C = \frac{N}{R_L f}\left[\frac{\eta}{1-\eta-\frac{V_t}{V_{in}}}\right] \tag{3}$$

where η is the efficiency of the charge pump. This is inherently limited by the need for a positive capacitance, so:

$$\eta < 1 - \frac{V_t}{V_{in}} \tag{4}$$

The value of the output capacitor is dictated by the permissible level of ripple. It is given by:

$$C_{out} = \frac{1}{\alpha f R_L} \tag{5}$$

where α is the ripple allowed in the output voltage as a fraction of the mean output voltage.

C. Specific Charge Pump Design

The basic specifications call for the LED to light up when 10dBm of power is supplied. This power is delivered via a 50Ω line, and so is equivalent to an RMS voltage of $0.7071V$. The turn-on voltage of the provided RF Schottky diodes (Avago HSMS-2862's) is approximately $0.3V$[1], and the provided LED turn-on voltage is approximately $1.7V$. Thus equation 2 gives a minimum value for N of 4. However, there is a tradeoff to be made here: using the minimum permissible value for N will result in the lowest possible loss while meeting the basic specifications, but will cause the LED to cease illuminating at a higher input power (but less than 10dBm) than if a higher value for N is used. Of course as the input power drops too low, then the system will not be able to provide sufficient current to drive the LED, no matter how high the theoretical voltage across the load. As a compromise, a value of N=5 is used for this work (with the option of switching to N=6 built into the fabricated designs).

In order to determine the optimal capacitor values, it is necessary to know the load impedance. In this case, the load is a diode, so the impedance changes with voltage. This means that load impedance will change from when the circuit is first turned on until it reaches steady state. The I-V curve for the LED was measured, and is plotted in figure 3. Around turn-on voltage, the impedance of the LED changes rapidly, so for design purposes a wide range of impedances could be considered optimal. A value of 800Ω is assumed here - this is approximately the measured value at 1.70 V.

The value of η is limited to 0.57 by equation 4. However, in order to achieve this value, very large capacitors would need to be used. Unfortunately, at frequencies of 5.8 GHz, the available 603 surface mount capacitor values are seriously restricted. The highest values found that were not self resonant at 5.8 GHz where 7 pF capacitors from ATC's 600S series[2]. This dictates a maximum possible efficiency of 0.499.

Ripple voltage is not a particularly serious concern for this project - variations of the brightness of the LED at 5.8 GHz are unlikely to be particularly noticeable to human observers. Somewhat arbitrarily, it was decided that a figure of 10% would be reasonable. Equation 5 then leads to a desired output capacitor of $2.155pF$.

A simple ADS simulation was created to check the basic

[1]from models of the diode included in the libraries of LTspiceIV and ADS 2008 update 2.

[2]other than the 850 pF DC blocks provided in class - problems simulating such large values resulted in them not being used

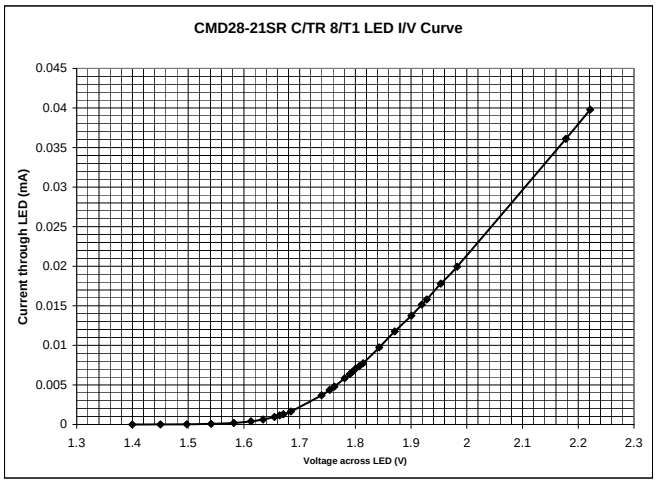

Fig. 3. The measured I-V curve for the LED used.

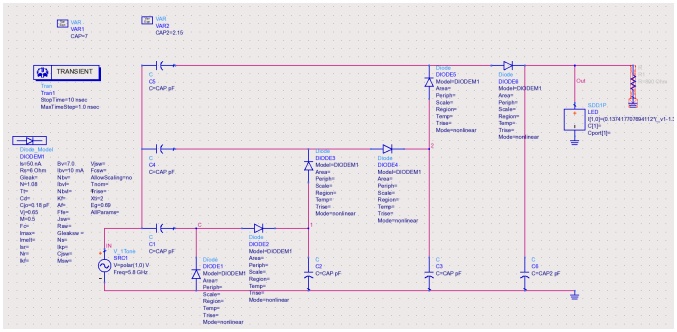

Fig. 4. The schematic used to simulate the behavior of the basic charge pump. Schottky diode parameters are those for the Avago HSMS-2862 [2]. LED model is based on measurements made for this report.

veracity of these numbers. The layout for this simulation is shown in figure 4, and the resultant output voltage is shown in figure 5. A model for the LED was implemented in ADS by using a 1-port network with a current related to voltage by a 6th order polynomial fit to the diode I-V curve in figure 3, and the voltage generated across this is also included in figure 5.

III. Power Divider Design

The charge pump design outlined in the preceding section requires the incoming signal to be divided into three. Initial implementations involved simply splitting the power with a microstrip cross and two corners (basic design in figure 7). In simulation this works, but the power output is below optimal at 5.8 GHz. From figure 7 it can be seen that, at least with the cascaded-Wilkinson type power divider, improved power throughput was achieved.

There are many different designs for three-way power dividers in the literature, several of which are listed by [3]. Many of these would present considerable difficulties in coming up with a workable a layout, but attempts were made to implement both the design outlined in [3] and that in [4]. [3] simulated well as a schematic (see figure 6). Unfortunately

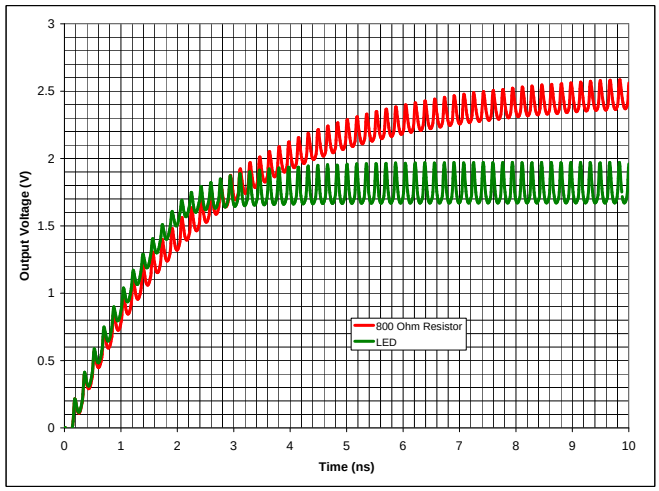

Fig. 5. The output voltage from the charge pump as a function of time from initial switch-on. Shown for both an 800 Ω resistor (the assumed impedance at the operating voltage) and for a model of the LED. It can be seen that since the LED's impedance drops off rapidly with increasing voltage the voltage across the LED effectively gets stuck a little above turn-on. If more current were available, this would occur at a higher voltage.

however, trace width constraints made the implementation of the [3] design impossible. A possible implementation of the [4] design was devised, and is shown in figure 7 (Goldfarb), but the performance was not as good as hoped. In an effort to improve performance and simplify the design, it was decided to implement a version using cascaded Wilkinson power dividers. The basic idea was to first split the signal equally in two, and then split each of the resulting signals in two again, with 2/3 of the power from each signal going directly to the charge pump and the two remaining thirds recombined using a third (equal split) power divider. The output impedance of an equal split Wilkinson power divider is the same as that of the input [5] (in this case, 50Ω). However, this is not the case for non-equal split power dividers. As a result, 1/4 λ matching networks were included between the 1/3 and 2/3 arms of the unequal power divider and the recombining Wilkinson and charge pump, respectively. It was found in simulation that the matching network between the 1/3 arms and the recombining Wilkinson did little to improve overall performance, so this was removed, shortening the overall length of the power divider.

It was also found that the very thin traces for the 2/3 1/3 power divider were not achievable with in-house manufacturing, so instead a 40:60 split was used. This results in slightly more power in the central output than desired, as can be can be seen in figure 7. This should not be a problem: assuming equal impedance at each of the capacitor inputs to the charge pump, it will result in different voltages at each capacitor, at least at the very start of a cycle. However, as it progresses the voltages across each capacitor will change differently, resulting in different impedances offered at each input, in turn leading to different voltages across each capacitor. This is expected to gradually even out the voltages across each stage.

It should be noted that while both the Goldfarb and

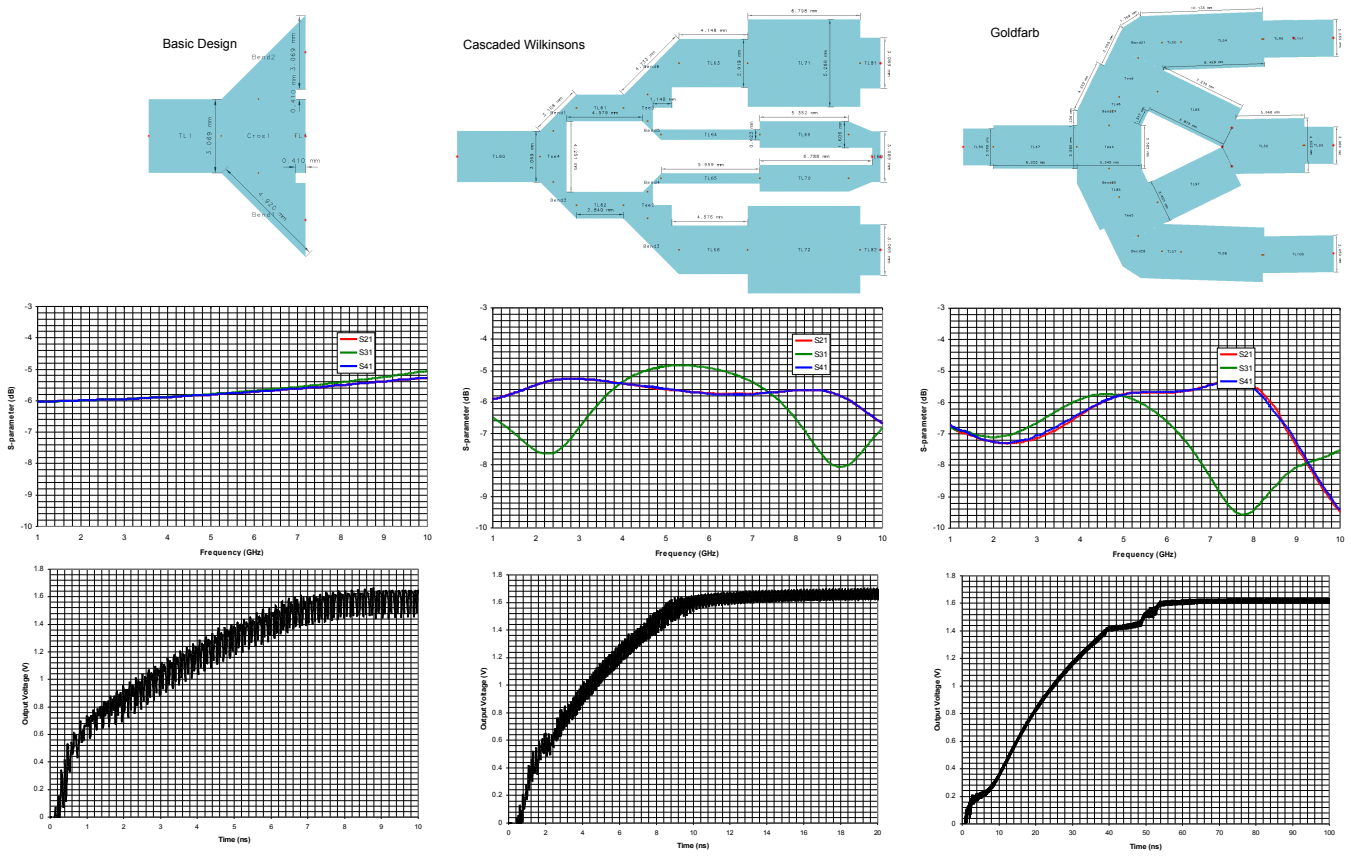

Fig. 7. Simulated layouts considered. The center (cascaded Wilkinson) design was the one chosen for implementation. The center row of plots shows the s-parameters for each layout, as simulated in Momentum. The lowest row of plots shows the effect on the output voltage across the LED for each layout. These results are from ADS simulations. It can be seen that the two 'proper' power divider circuits take longer to reach that steady state, but perform somewhat better once they get there. All of these designs assume the use of 62 mil FR-4 as the substrate, and further assume a dielectric constant of 4.34.

cascaded-Wilkinson designs should nominally incorporate several resistors, these have been left out of the designs. The resistors are there to improve isolation between ports 2 and 3, something that is not necessary here.

Several matching schemes were considered for these layouts. It was found that the real part of the input impedance to the circuits was too low to permit the use of stepped-impedance matching networks, and so stub or lumped-element matching were thought to be the next best options. There was some uncertainty as to the accuracy of the ADS S-parameter simulations used to determine input impedance, due in large part to the non-trivial time dependence of the circuit behavior. It was considered best to simply allow sufficient space on the input line to the circuits to permit a matching circuit to be constructed based on measured impedance, if necessary.

IV. Final Implemented Designs

Shortly prior to submitting these designs for manufacture, it was discovered that the substrate to be used was 31 mils thick, and not the 62 mils assumed in all designs. As a result, it was necessary to rapidly modify the cascaded-Wilkinson type power divider to work on this substrate. At the suggestion of the manufacturer, the assumed dielectric constant of the FR-4 was changed to 4.8 for these designs. Two different layouts were produced, both of which are shown in figure 8. In simulation narrower (primary) layout was found to perform somewhat better than the wider (secondary) layout (see figure 9, but it was considered possible that coupling between traces would be more of an issue than was apparent in simulation, so the wider version was also implemented.

As can be seen from the layouts (figure 8), additional vias and traces were added to the board to allow the optional increase of the order of the board from 5 to 6. It was considered prudent to include this since only a single attempt at manufacture was possible. This should not in any way affect the performance of the N=5 version. It was hoped that this would allow recovery from some possible systematic errors in the simulation.

V. Results

The devices were fabricated and populated as shown in figure 10, and both were found capable of lighting the LED with a 10 dBm input, and indeed with an input down to around 3-5 dBm (depending on precisely what level of light emittance the LED is considered to be on). In the primary device, a voltage of 1.626 V was produced across the LED with a 10dBm input, while 1.638 V was produced with the secondary device. Both are somewhat lower than the specified

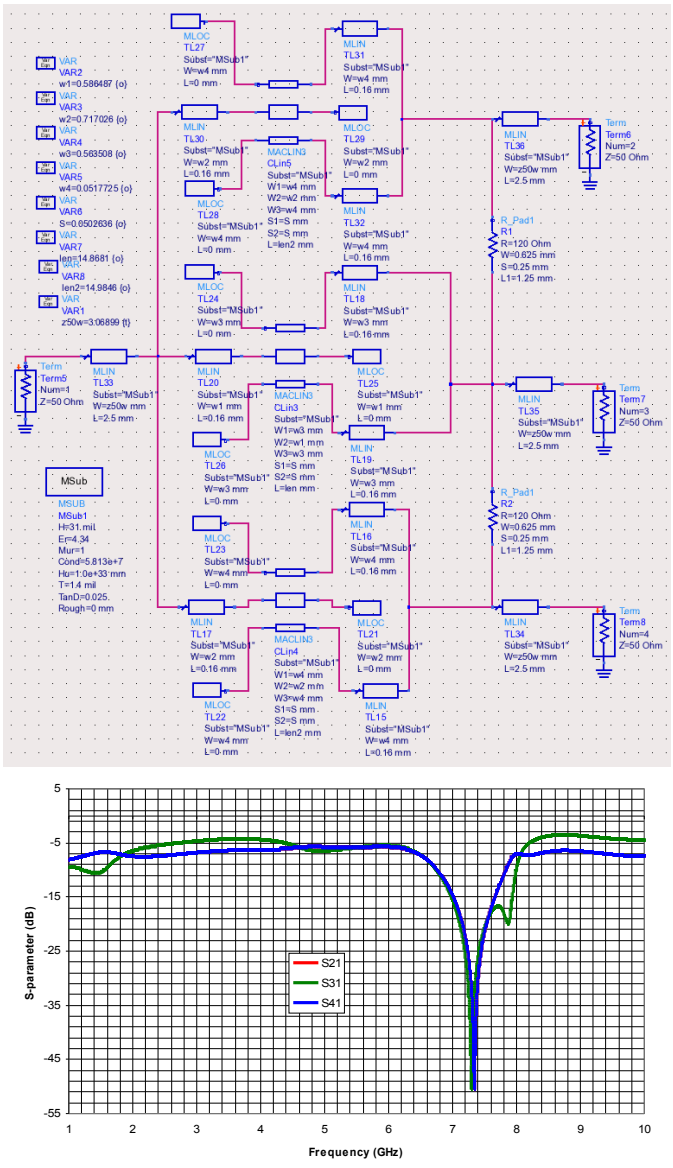

Fig. 6. Schematic and simulation results for the Chiu style power divider. This design offered excellent performance with in very short length ($1/4\lambda$), but required trace widths and separations to small for the in-house manufacturing processes to be used.

turn-on voltage for the LED, but were sufficient to turn the LED on.

Some attempts were made to improve the matching of the primary design by adding grounded lumped-element capacitors and inductors as well as open stubs to the input line to the coupler, but no improvement in performance was observed. As can be seen from figure 11, the matching of both devices is already fairly good without additional components being added. Furthermore, the devices both met all specifications without the addition of a matching network. As a result, attempts to improve matching were abandoned.

The voltages are somewhat lower than those found in simulation. This can be attributed in part to the capacitors used in the final design: a delay in shipping resulted in 4.7 pF capacitors being used rather than the desired 7 pF. Simulations

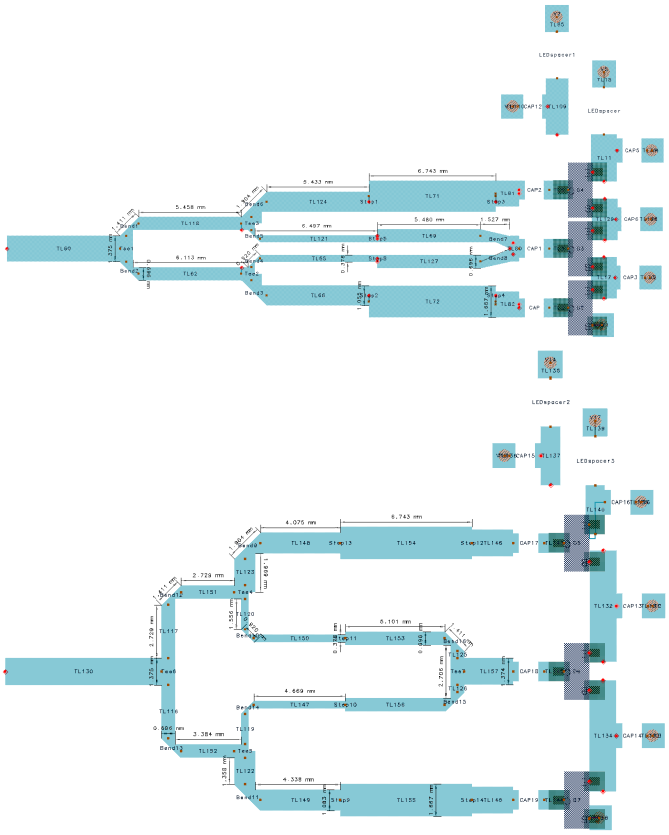

Fig. 8. The narrow (primary) and broad (secondary) designs submitted for manufacture.

suggested that this would result in a lower output voltage. It is also likely that the hand-soldering introduced losses not included in the simulations. Furthermore, the designs were fabricated with some dimensions (particularly those on the mitered corners) very close to the manufacturing tolerances. Visual inspection suggests that the trace at at least one of these corners is slightly broken. The break is evidently not large enough to badly affect performance, but may well introduce some additional loss.

It is of note that the relative performance of the two devices are the reverse of that expected from power-divider simulation. It seems likely that this is due to the secondary design (by chance) being closer to matched to 50 Ω than the primary, as can be seen in figure 11. The N=5 versions of the design were found to meet the requirement, but it was decided to also test the 6th order version. This did not improve performance at all - in fact, the voltage across the LED dropped slightly. It can be concluded that the limiting factor in performance is not voltage, but current draw. Not enough power is being supplied to the LED (in either N=5 or N=6 configuration) to allow the desired 1.7 V. Performance improvements would therefore have to come from reduced loss, and perhaps better matching.

VI. Conclusions

The manufactured devices successfully met all of the requirements. Further improvements in performance are likely

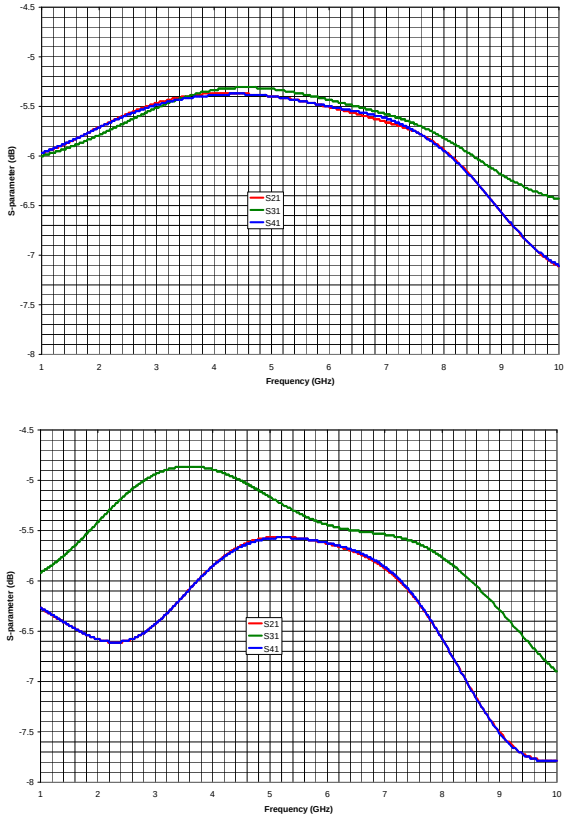

Fig. 9. The simulated performance of the two implemented power dividers.

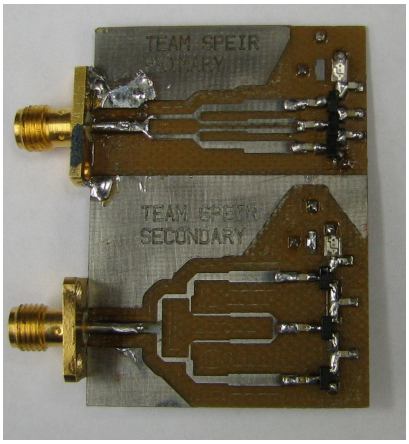

Fig. 10. The two implemented designs.

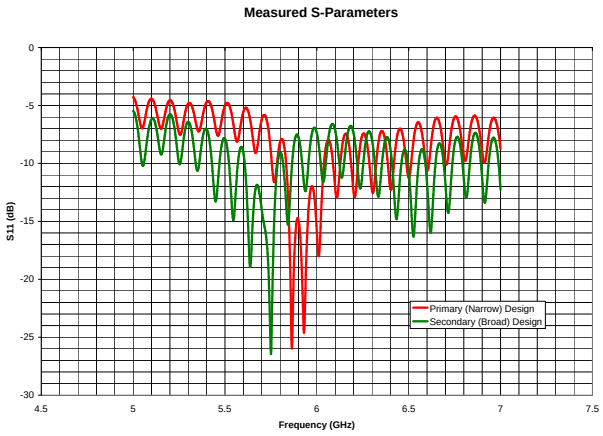

Fig. 11. The measured S_{11} for the two implemented layouts.

Component	Quantity	Cost Per Unit	Total Cost
Avago HSMS-2862	3	$ 0.62	$1.86
LED (CML CMD28-21SR)	1	$ 0.31	$ 0.31
AVX 2pF Cap (SQCSVA2R0BAT1A)	1	$ 0.646	$ 0.646
AVX 4.7pF Cap (SQCSVA4R7CAT1A)	5	$ 0.476	$ 2.38
SMA Connector	1	?	?
FR-4 Board	1	?	?
		Total:	$ 5.20

TABLE I
BILL OF MATERIALS.

to come through the use of higher value input capacitors, and potentially also by the use of a better power divider. It is probable that the brightness of the LED at 10dBm input could be improved through use of a lower-order charge pump, but this would be at the expense of any illumination at all at lower frequencies.

A list of the parts used in the final designs) and associated costs is shown in table I. The table lists quantities for either one of the designs. Both designs use the same components (although the secondary design uses a slightly larger area of FR-4). Costs are based on the unit cost for the purchase of the smallest possible number of components from Digikey (www.digikey.com), as of 7/21/2009.

REFERENCES

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[3] J.-C. Chiu, J.-M. Lin, and Y.-H. Wang, "A novel planar three-way power divider," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 8, pp. 449–451, 2006.
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