5.8 GHz Charge Pump Receiver

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I. Introduction

The number of RF signals pervading urban and suburban areas today presents a non-trivial amount of power compared to the consumption of many modern digital devices. Such RF power has been identified as a potential source to drive some simple circuits, similar to the methods RFID technology uses. Such advancements represent a great step forward for many industries related to digital design by decreasing costs related to power supply components and eliminating batteries or the need to connect to external power.

One of the greatest challenges to implementing this method is transforming the signals into a DC voltage that can be used by some digital component. This is more easily accomplished with passive components since any active components would have to draw power from the time-varying RF signal. In this study, capacitors and diodes are assembled to create a charge pump capable of producing the turn-on voltage of an LED given an input signal of 10 dBm at 5.8 GHz. This demonstrates the possibility of a simple and effective method of RF power scavenging for low-power computation.

II. Design and Simulation

A. Topology and Initial Calculations

The well-known charge pump circuit arrangement given in Figure 1 was chosen because of its simplicity to implement and analyze. The circuit acts as a voltage doubler with the ability to easily chain stages together. When the signal has negative polarity, current is pulled through the grounded diodes, causing some charge to be stored in the series capacitor. With positive antenna voltage, the series capacitor discharges, adding a voltage wave to the antenna's excitation. The shunt capacitor then charges up, discharging when the source polarity again switches. This results in about twice the peak voltage delivered by the antenna for each stage since the negative peak has been rectified and added in phase with the positive peak.

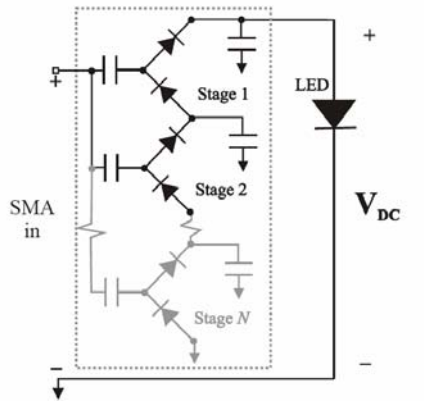

Fig. 1. Multi-stage voltage doubler scheme to power LED.

Each negative and positive peak of the antenna signal must overcome the diode turn-on voltage. The DC voltage observed at the output can then be calculated as

$$V_{DC} = N\left(V_A - V_T\right),$$

where N is the number of stages, V_A the peak voltage from the antenna, and V_T the turn-on voltage of each diode. To achieve the LED turn-on voltage of 1.7 V using Schottky diodes with V_T = 0.5 V, at least two stages are needed, corresponding to two pairs of diodes and capacitors. However, this calculation assumes perfect matching between the circuit and the antenna (so that the antenna provides 1 V peak), matching between the transmission lines and diodes, and negligible losses in the transmission lines. Because of the incertitude of these assumptions, more stages were expected necessary in implementation.

B. Components

The components chosen for this circuit are listed in Table 1. The LED drew a forward current of about 1 mA when supplied with the turn-on voltage of 1.7 V. The Schottky diodes, which were packaged in series pairs in SOT-23 packages, drew between 10 and 20 mA when supplied with forward voltages between 0.4 and 0.5 V. Dielectric Laboratories was chosen as the source of capacitors because of the high self-resonance frequency of their C06 line.

Table 1. Charge Pump Components

Component	Manufacturer	Model #
LED	CML	CMD28-21
Schottky Diode	Avago	HSMS-2862
Capacitors	Dielectric Labs	C06 series

C. Simulation Results

The substrate parameters summarized in Table 2 were used in ADS simulations of the circuit. 32 mil FR4 was chosen because it allowed for smaller trace widths than 62 mil substrate, and no thinner substrate was available through the in-house fabrication facilities employed for this project.

Table 2. Charge Pump Circuit Substrate Parameters

Parameter	Value
Substrate thickness	32 mil
Relative permittivity	4.2 @ 6 GHz
Conductor conductivity	5.813×10^7 S/m
Metallization thickness	1 mil
Loss tangent	0.02

The circuit layout was considered first so the simulation schematic would more accurately represent the output voltage behavior. The internal ADS model for the HSMS-2862 Schottky diode package was identified. Ideal capacitors were assumed. Three stages were included in accordance with the expectation that the minimum two calculated before would not be sufficient; the option of adding a fourth stage was added to the layout. The LED was excluded, a suitable ADS model not having been found and the corresponding data sheet missing necessary information to construct a model. In the simulation schematic, it was modeled as a 1mA current source since that was the forward current seen in the device with a forward voltage of 1.7 V.

While designing the layout (shown in Figure 2), the circuit size, trace lengths, and input signal strength were major considerations. The weak signals from the antenna (whose input impedance was uncertain but was expected to be near 50 Ω) meant that loss in traces had to be minimized. Therefore, power splitting among the four stages was accomplished by four simple T-junctions. Although an equal-split power divider could have been constructed, it would greatly increase the size of the circuit and lengths of traces. Four-way junctions were avoided because of the extra parasitic capacitance and loss associated with them compared to T-junctions. Matching between the diode packages and 50 Ω was not included in initial simulations because of the loss incurred in matching networks and the possibility of its superfluity.

An ADS simulation schematic was generated from this layout to perform simulations since they could be conducted more quickly in that form. Performance expectations were based on these simulations since the layout was designed for the traces to have little effect.

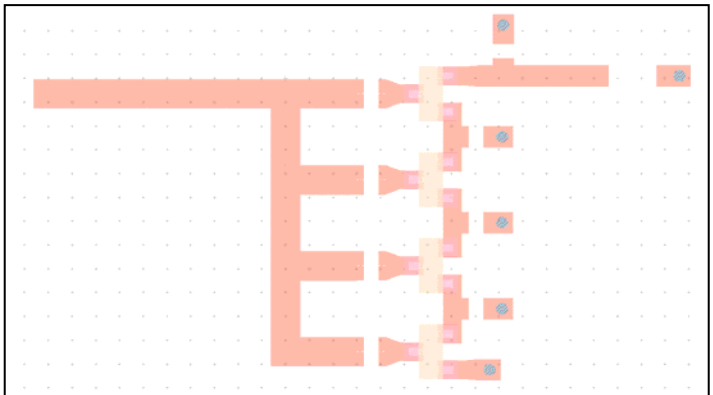

Fig. 2. Layout for charge pump circuit.

A transient simulation was conducted to predict output voltage as a function of time. This allowed the ripple in the DC output to be observed as well as the capacitor charge time necessary to reach the turn-on voltage. After conducting several initial simulations, it was determined that increasing the series capacitances near the antenna increased the output voltage since more charge could be stored. Increasing the shunt capacitances near the LED reduced the ripple somewhat by shunting high frequency components, but capacitances larger than about 2 pF caused voltage to drop below optimal levels by providing a low impedance path to ground. Capacitances of 33 pF and 1.5 pF respectively were chosen based on these observations and the availability of these values in high frequency packages. The transient simulation result with these values is shown in Figure 3.

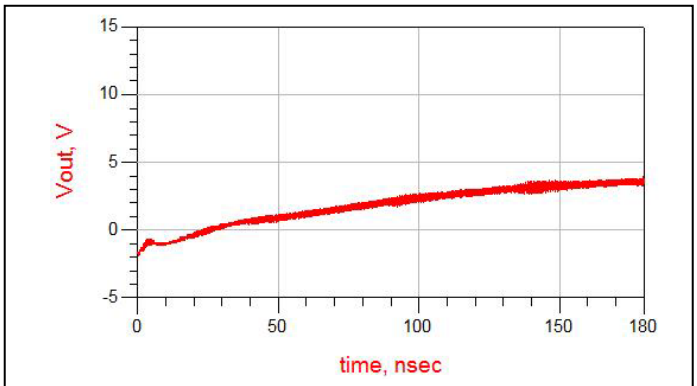

Fig. 3. LED voltage vs. time with final capacitance values.

The output voltage converges on a DC value of about 4 V with a 1 V ripple. This result is verified by the harmonic balance analysis result, which is converted to the time domain for Figure 4. Although this high level of performance was not expected in the actual circuit, the degree of over-design observed in these results was considered sufficient to proceed with fabrication of the Figure 2 layout.

Frequency domain and Smith chart plots of s_{11} are given in Figure 5. Despite the somewhat high reflection at 5.8 GHz, the frequency profile of antenna impedance was unknown, so input matching was still ignored. All attempts that were made to match the diode input to 50 Ω resulted in an inferior *s*-

parameter response, so matching at these locations was not executed either. As expected, the input impedance has a large capacitive component.

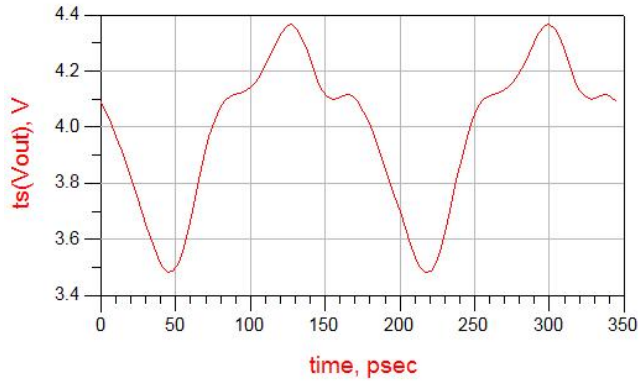

Fig. 4. Harmonic balance analysis result for output voltage, converted to time domain.

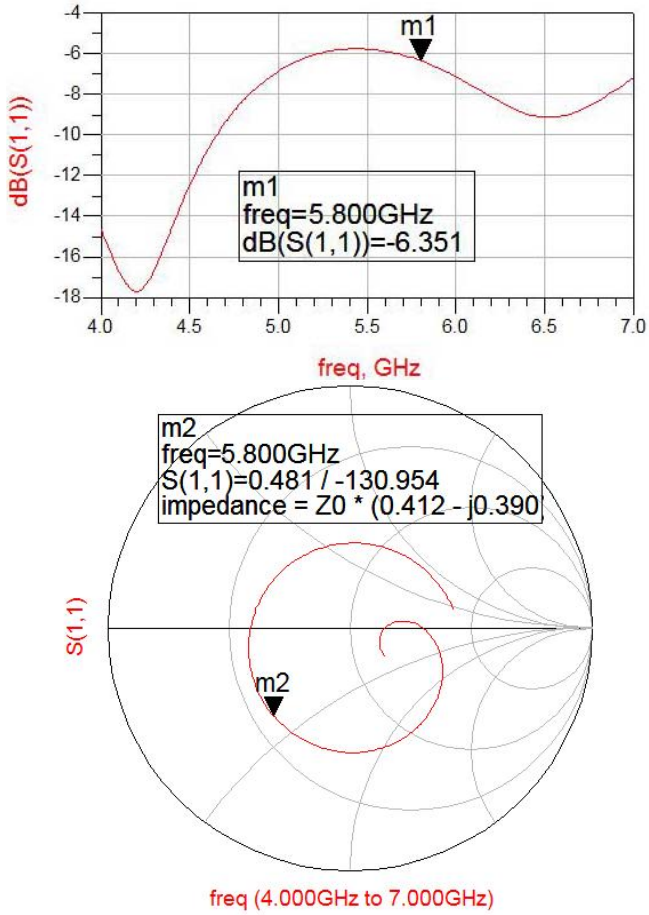

Fig. 5. Frequency domain and Smith chart plots of s_{11}.

III. Fabrication and Results

The charge pump circuit was fabricated at in-house facilities with no apparent errors. Because the equipment did not provide for plated-through vias, short solid wire sections were inserted and soldered to the top and bottom of the board to provide ground connections. The completed board with components for three stages is shown in Figure 6.

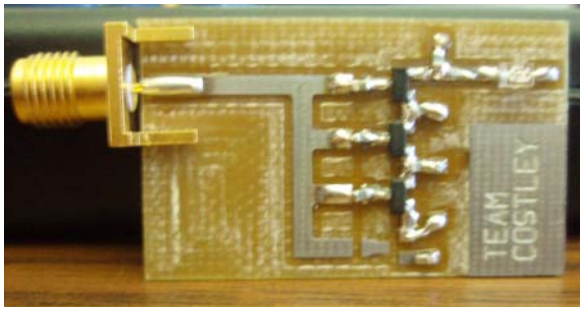

Fig. 6. Completed charge pump circuit with three stages assembled and hand-soldered.

The LED was found to illuminate with an input signal of 10 dBm as specified (see Figure 7). The average DC voltage across the LED with this input was measured to be about 1.8 V, although some high-frequency ripple was likely present. The LED was in fact found to illuminate with an input power as low as -0.5 dBm albeit very dimly. That the device surpassed the specification by so much is attributed to the overdesign of the circuit during simulation and the attention to loss in the circuit layout.

Fig. 7. LED illuminated in a dark room with 10 dBm input signal.

The circuit's s_{11} data as measured by the network analyzer is given in Figure 8. The reflection at 5.8 GHz is slightly better than predicted by the ADS simulation, and although there is still room for optimization, the device still outperformed specifications.

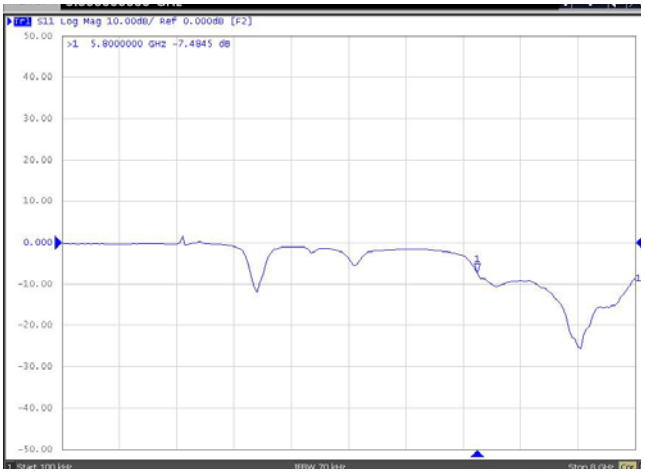

Fig. 6. VNA measurement of s_{11} (-7.485 dB at 5.8 GHz).

IV. Conclusions

The charge pump greatly exceeded specifications by illuminating the LED with an input signal of only -0.5 dBm. The circuit was intentionally designed as simply and compactly as possible, forgoing more complex networks to preserve as much input power as possible. This approach also reduced the probability of the fabricated circuit exhibiting unexpected behaviors departing from the simulation.

References

[1] D. M. Pozar, "The Wilkinson Power Divider," in *Microwave Engineering*, 3rd ed. Hoboken: John Wiley, 2005, pp. 318–323.

Bill of Materials

Item	Part Number
LED x1	CMD28-21
Schottky Diode x3	AV02-1388EN
33 pF cap x3	C06CF330J-9ZN-X1T
1.5 pF cap x3	C06CF1R5B-9ZN-X1T
SMA connector	30 mil board side mount
30 mil FR4 circuit board	In-house fabrication

Appendix: Dimensioned Charge Pump Layout