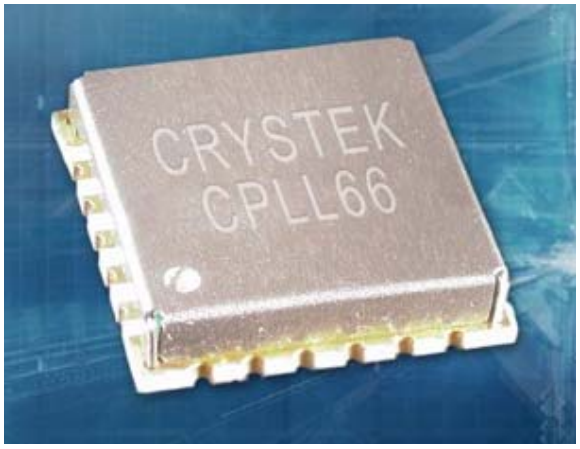
Crystek Crystals Corporation
Quality Products & Superior Service Since 1958

RF PLL Synthesizer



Features

1GHz-5GHz Range

Standard 3 Wire Interface

Small layout 0.6" x 0.6"

Applications

Digital Radio Equipment
Fixed Wireless Access
Satellite Communications Systems
Base Stations
Personal Communications Systems
Portable Radios
Test Instruments
Wireless Infrastructure

The CPLL66 is a complete PLL/Synthesizer needing only an external frequency reference and supply voltages for the internal PLL (phase lock loop) and VCO (voltage controlled oscillator). The Crystek CPLL66 is programmed using a standard three line interface (Data, Clock and Load Enable).

The newly introduced CPLL66 family has been initially released to cover 1GHz to 5GHz in bands. It is housed in a compact 0.6-in. x 0.6-in. x 0.15-in. SMD package which saves board space. Typical phase noise at 4GHz is -90dBc/Hz at 10KHz offset with 0dBm minimum output power.

Crystek Crystals Corporation 12730 Commonwealth Drive • Fort Myers, FL 33913
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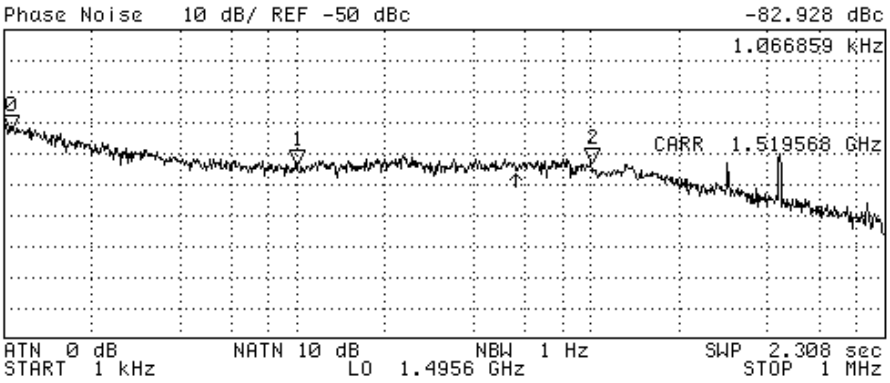
CPLL66-3160-3380
0.60" SQ SMD

RF PLL Synthesizer

PERFORMANCE SPECIFICATION	MIN	TYP	MAX	UNITS
Frequency Range:	3.16		3.38	GHz
Step Size		2500		KHz
Settling Time		3		msec
Output Power:	0	3	6	dBm
Output Phase Noise				
@1KHz offset		-90	-85	dBc/Hz
@10KHz offset		-95	-90	dBc/Hz
@100KHz offset		-115	-110	dBc/Hz
@1MHz offset		-135	-130	dBc/Hz
Power Supply				
V1=VCO Supply	4.75	5	5.25	Volts
V2=PLL Supply	2.7	3	3.3	Volts
Supply Current				
I1=VCO Input Current		50		mA
I2=PLL Input Current		25		mA
Spurious Suppression				
PFDSpur		-70	-60	dBc
Reference Feedthru		-80	-70	dBc
Harmonic Suppression (2nd Harmonic):				
2nd		-15	-10	dBc
3rd		-25	-15	dBc
Reference Frequency		10		MHz
RF Output Level	-5	0	5	dBm
Input Impedance		100K		Ohm
Rf Output Impedance		50		Ohm
Operating Temperature Range:	-40		85	°C



N	SWP PARAM	VAL
0	1.066859 kHz	-82.928 dBc
1	10 kHz	-94.406 dBc
2	100 kHz	-93.942 dBc

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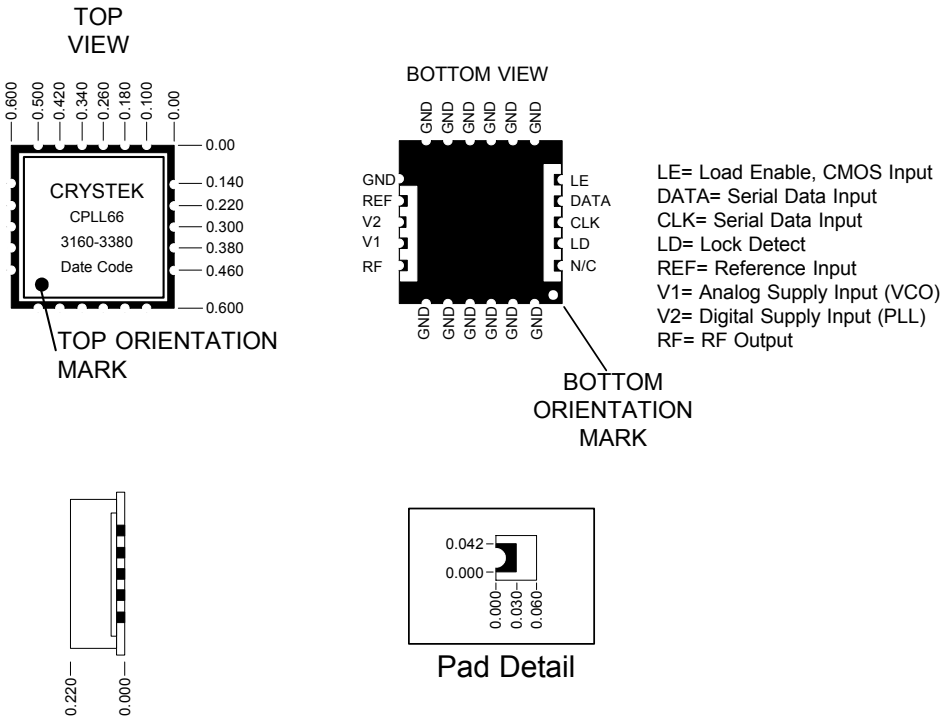
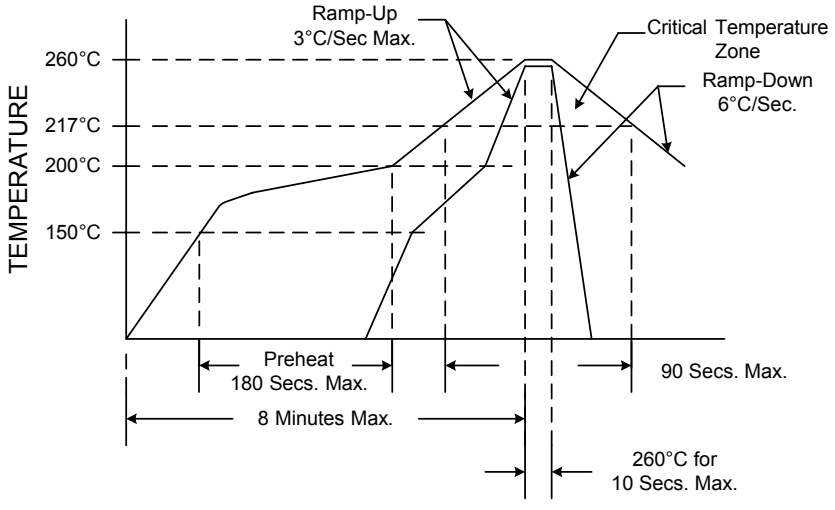


RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.

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ENVIRONMENTAL COMPLIANCE

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Programming Guide for CPLL66-XXXX

Introduction

The CPLL66 uses a simple 3 wire interface to program four internal registers. See Figure 1.

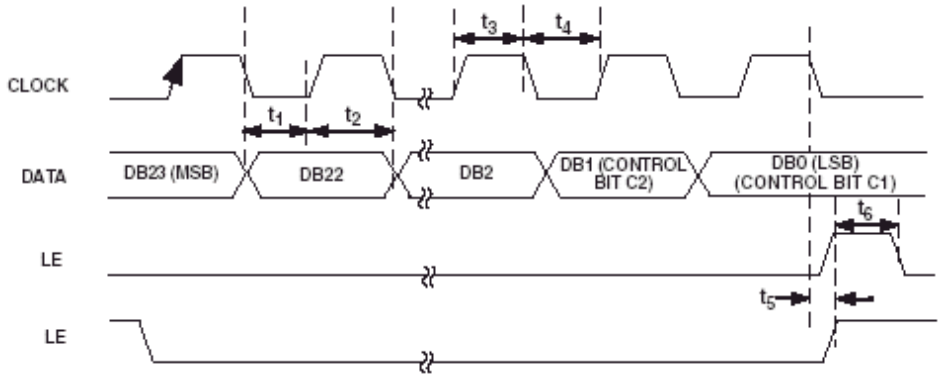

Figure 1. Timing Diagram

There are four 24 bit registers that need to be programmed. Which register is written into is simply controlled by Control Bits C1 and C2. Table I summarizes the Truth Table for Control Bits C1 and C2.

Table I. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

Table II shows the details of the four 24 bit registers.

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Table II. Latch Summary

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCLER VALUE		POWER-DOWN 2	CURRET SETTING 2			CURRET SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CP16	CP15	CP14	CP13	CP12	CP11	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCLER VALUE		POWER-DOWN 2	CURRET SETTING 2			CURRET SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CP16	CP15	CP14	CP13	CP12	CP11	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

When using the CPLL66 family in a synthesizer application, all four 24 bit registers need to be written into after power-up. After writing all four latches the first time, subsequent frequency step changes can be accomplished by changing the N Counter Latch only.

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Power Supply Sequencing

The CPLL66 family of synthesizers requires 2 power supplies to operate. These supplies are VCO Supply (V1) and the PLL Supply (V2). The PLL Supply V2, must be applied before the VCO Supply V1. In addition, the CLOCK, DATA and LE lines should not be active before the PLL Supply V2 has come up.

Programming Crystek p/n: CPLL66-3160-3380

The following is specific programming for CPLL66-3160-3380 (3.16GHz~3.38GHz with 2500KHz Step Size and 10MHz input reference frequency).
Program all four registers with the following:

Reference Latch: 000010 H
N Counter Latch: 002741 H
Function Latch: 800012 H
Initialization Latch: 000013 H

The above values will set the CPLL66-3160-3380 to 3.16GHz

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